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Delay Compensation Technique for CM EMI Mitigation in Power Inverters

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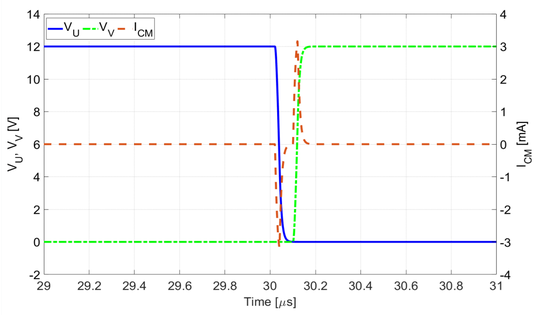
Research context and motivation

Power switching circuits generate high dV/dt and dI/dt edges, which are the main responsible for the generation of EMI, and in particular of common mode (CM) currents. Usually, these CM currents are attenuated adding filters at the PCB level, but they are expensive, heavy and bulky. Another solution is to use software techniques like slew rate control and waveform shaping, but they have many drawbacks on the circuit efficiency. This work has been focused to develop a new closed loop technique able to reduce the CM conducted emission, using a software solution, without affecting the dissipated power.

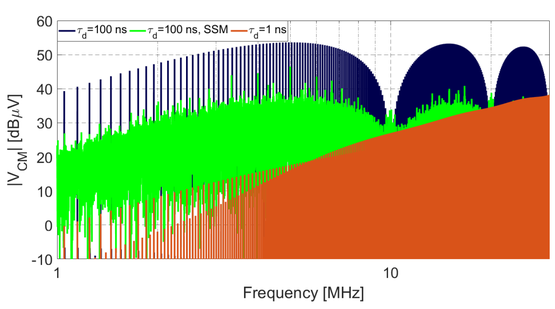
Addressed research questions/problems

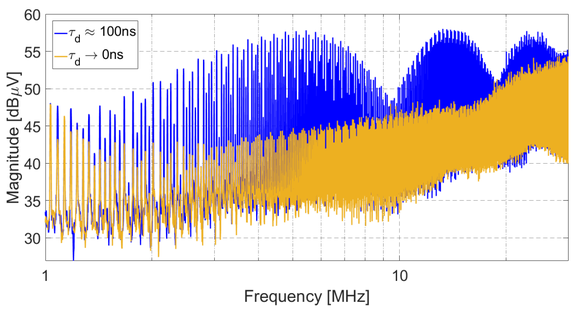
- The target application of this research activity is an inverter used to drive a BLDC motor. Such motor is controlled by three trapezoidal waveforms, shifted in phase by 120 degrees.
- The generation of CM emissions is mainly due to the pulsed current injection in the parasitic capacitances between the inverter board and the ground plane. Specifically, the output nodes of the inverter show high slew rate signals, which are the main responsible for the current injection in the parasitic capacitances.



Aiming to reduce the generation of this CM current it is possible to use a complementary PWM. Indeed, if the two output waveforms complement to one another, no CM current flows in the parasitic capacitances. However, the output voltage waveforms are not, since some delay (τ_d), due mainly to the drivers, is present between the waveforms at the two active output nodes. This delay generates CM currents. So, to mitigate these currents, the two output waveforms should be aligned.

- In order to define the relation between the time delay and the CM emission an analytical model has been developed. Moreover, Spice simulations have been carried out in order to compare the proposed technique with the Spread Spectrum Modulation (SSM). The proposed technique reduces the CM emission 10 dB more than SSM up to 24 MHz, with the aligning accuracy that can be reached by commercial microcontrollers. Over this frequency the two reduction techniques show similar performance.





- Some preliminary emission measurements on an inverter, aligning manually the output waveforms, have been carried out, confirming that the CM disturbance spectrum is reduced when the output waveforms are aligned. The attenuation magnitude reaches -15 dB [5].
- Given that the value of τ_d has an high uncertainty and it could vary during the inverter operation, a feedback control system is needed to ensure the minimum CM EMI generation in every working condition.

List of attended classes

- 01NKXNC – Controllo Digitale di Convertitori e Azionamenti (2017, 6 credits)
- 01RJLRV – Advanced control in electrical energy conversion (2017, 4 credits)
- 02LWHRV – Communication (2017, 1 credit)
- 08IXTRV – Project management (2017, 1 credit)
- 01RISRV – Public speaking (2017, 1 credit)
- 01QORRV – Writing Scientific Papers in English (2017, 3 credits)
- 02RHORV – The new internet society: the black box of digital innovation 1 (2017, 1 credit)
- 01SEZRV – Managing PhD thesis as a project (2017, 2 credits)
- 01LCPIU – Experimental modeling: costruzione di modelli da dati sperimentali (2018, 6 credits)
- 02ITTRV – Generatori e impianti fotovoltaici (2018, 5 credits)
- 01SFURV – Programmazione scientifica avanzata in Matlab (2018, 4 credits)
- 03AFINC – Azionamenti Elettrici (2019, 10 credits)
- 01SHMRV – Entrepreneurial Finance (2019, 1 credit)
- 01TETRU – Forensic Metrology (2019, 4 credits)
- 01SYBRV – Research integrity (2019, 1 credit)
- 01SWQRV – Responsible research and innovation, the impact on social challenges (2019, 1 credit)
- 01SWPRV – Time management (2019, 1 credit)

Submitted and published works

[1] M. Perotti and F. Fiori, "*Software based control of the EMI generated in BLDC motor drives*", EMC Europe 2016, Wroclaw, 2016.

[2] F. Fiori and M. Perotti, "*On the Use of the IC Stripline to Evaluate the Susceptibility to EMI of Small Integrated Circuits*", EMC Europe 2016, Wroclaw, 2016.

[3] M. Perotti and F. Fiori, "*Reduction of the EMI in BLDC Motor Drives Based on Delay Compensation*", SIE Meeting 2017, Palermo, 2017.

[4] M. Perotti and F. Fiori, "*A Test Structure for the EMC Characterization of Small Integrated Circuits*" in IEEE Transactions on Instrumentation and Measurement, vol. 67, no. 6, pp. 1461-1469, June 2018.

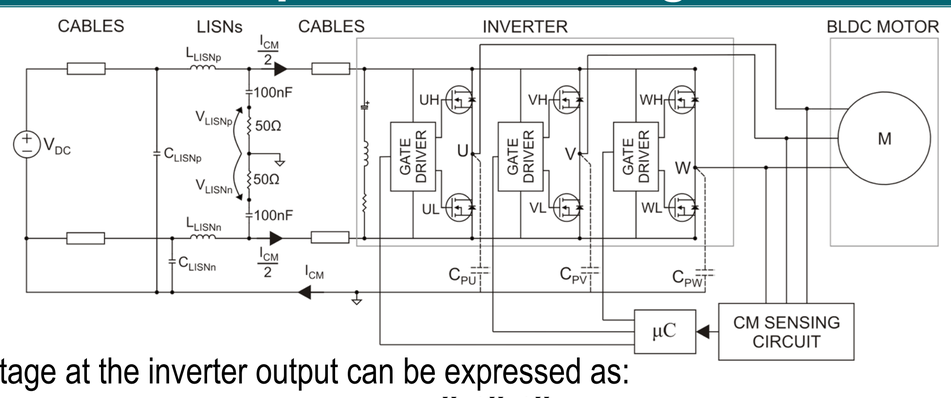
[5] M. Perotti and F. Fiori, *"Investigating the EMI Mitigation in Power Inverters Using Delay Compensation"* in IEEE Transactions on Power Electronics, vol. 34, no. 5, pp. 4270-4278, May 2019.

[6] M. Perotti and F. Fiori, *"Common Mode EMI Mitigation in Power Inverters Using Output Delay Compensation"*, PEAC 2018, Shenzhen, 2018.

[7] M. Perotti and F. Fiori, "*A Software Solution to Mitigate the EM Emissions of Power Inverters*", SIE Meeting 2019, Roma, 2019.

[8] F. Fiori, M.V. Quitadamo and M. Perotti, "*Novel Solutions to Reduce the Conducted Emissions of Power Switching Circuits*", EMC Compo 2019, Haining, Hangzhou, 2019.

Adopted methodologies



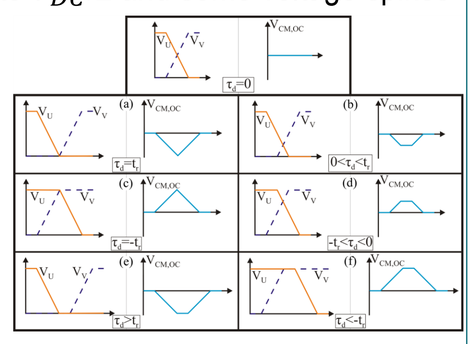
The CM voltage at the inverter output can be expressed as:

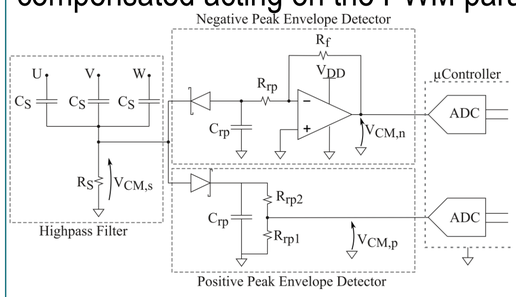
$$V_{CM} = \frac{V_U + V_V + V_W}{3}.$$

This voltage is the superposition of a DC component equal to $V_{DC}/2$ and some voltage spikes dependent on τ_d, which are the responsible of the CM EMI. The amplitude of these voltage peaks is proportional to τ_d when the delay is lower than the rising/falling time:

$$V_{CMpk} = \frac{V_{DC}}{3}\frac{\tau_d}{t_r}$$

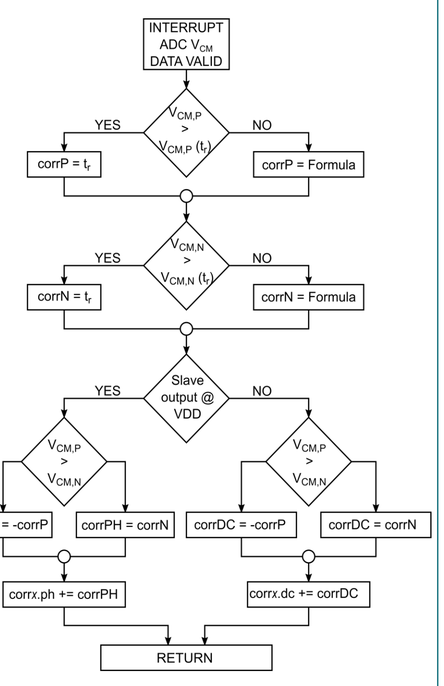
When $\tau_d > t_r$ this voltage saturates at $\frac{V_{DC}}{3}$. This peak value can be measured and therefore the delay can be compensated acting on the PWM parameters.

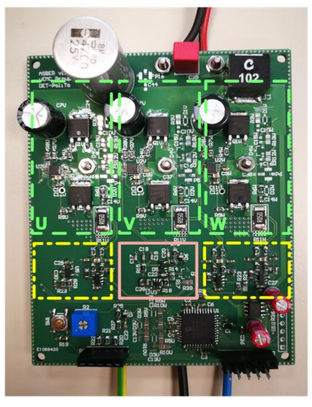




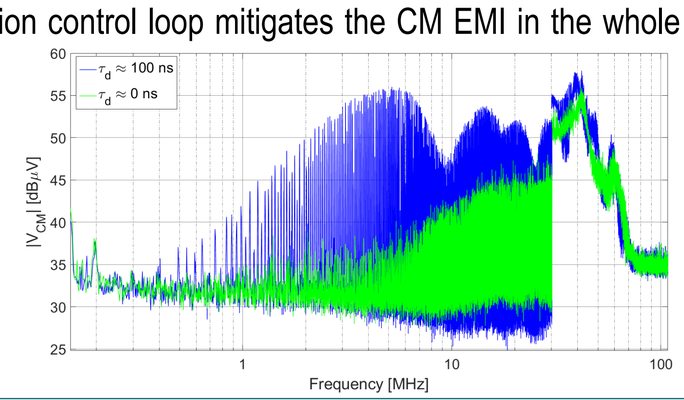
In order to sense the peak magnitude of these spikes, a signal conditioning network has been designed. Such network consist of three capacitors connected to the three inverter outputs respectively, and terminated on a resistance, obtaining an high-pass filter for CM.

The filter output voltage is given as input to two envelope detectors, one for the positive peaks and one for the negative ones. The peak is therefore sampled by two independent ADC channels of the microcontroller. A control state machine algorithm, whose flow chart is shown in the figure, modifies the PWM phase and duty cycle parameters, with a resolution of ~1 ns, aligning the output waveforms. A prototype of the inverter with the delay compensation system onboard has been designed and produced.





The conducted emission measurements have been performed on the system in two cases: the first, with the delay compensation control loop is deactivated, i.e. $\tau_d \approx$ 100ns; the second, where the control loop was activated, meaning with τ_d compensated. It can be seen that, from 150 kHz to 30 MHz, the delay compensation control loop mitigates the CM EMI in the whole frequency range, with a maximum reduction of 17 dB at 4 MHz. This result has been obtained without CM filter. In the frequency range from 30 MHz to 108 MHz the technique is not as efficient as in the lower part of the spectra, but the emissions are not worsened.



Novel contributions

- In this research activity the generation of the conducted CM emissions has been analyzed in detail, with analytical models including the time delay effect on EMIs.
- The technique has been applied on a three phase system driving a BLDC motor. It has been verified by measurements that, driving a BLDC motor, a proper alignment of the output waveforms can reduce significantly the CM disturbance level.
- A novel system, able to reduce in closed loop the CM EMI, has been designed, prototyped and tested. This system is composed of a low cost network and a software algorithm able to align the output waveforms. The proposed technique does not affect the system efficiency.

Future work

- Since SSM and signal aligning technique act with two different and uncorrelated principles, it would be possible to employ both techniques to obtain better performance.

POLITECNICO DI TORINO

PhD program in

Electrical, Electronics and Communications Engineering