

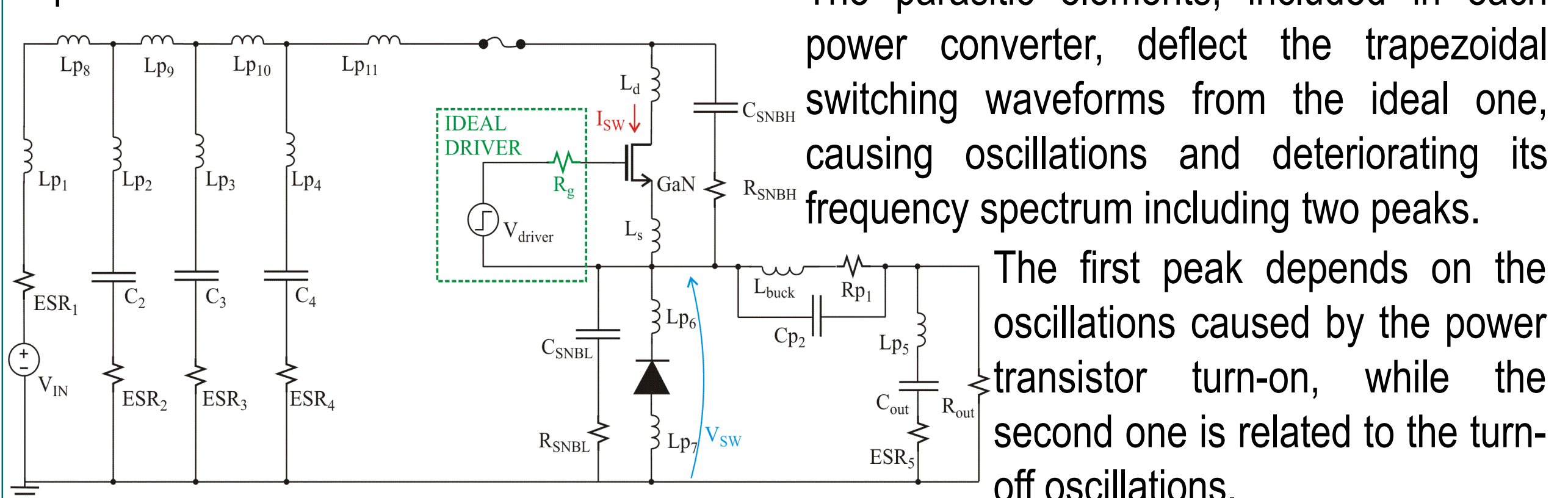
Research context and motivation

In recent years, wide bandgap semiconductors have become more popular in power electronics due to their higher efficiency and speed with respect to traditional silicon devices. Power converters, developed using these devices, exhibit higher dv/dt and di/dt which may excite high frequency resonant parasitic circuit, causing oscillations. As a consequence, the electromagnetic compatibility (EM) performance are worsen and over-currents and/or over-voltages could damage permanently the components of the circuit. The traditional approach to overcome these issues consists of placing an RC snubber in parallel to the switching nodes and a fixed value resistance between the gate terminal of the transistor and the driver. Such solution leads both to the introduction of other components in the circuit and to increase excessively the power dissipation. In order to address such issues, a mathematical method was extrapolated to optimally damp the oscillations and a current driving technique, allowing to reproduce the obtained results, was proposed.

Addressed research questions/problems

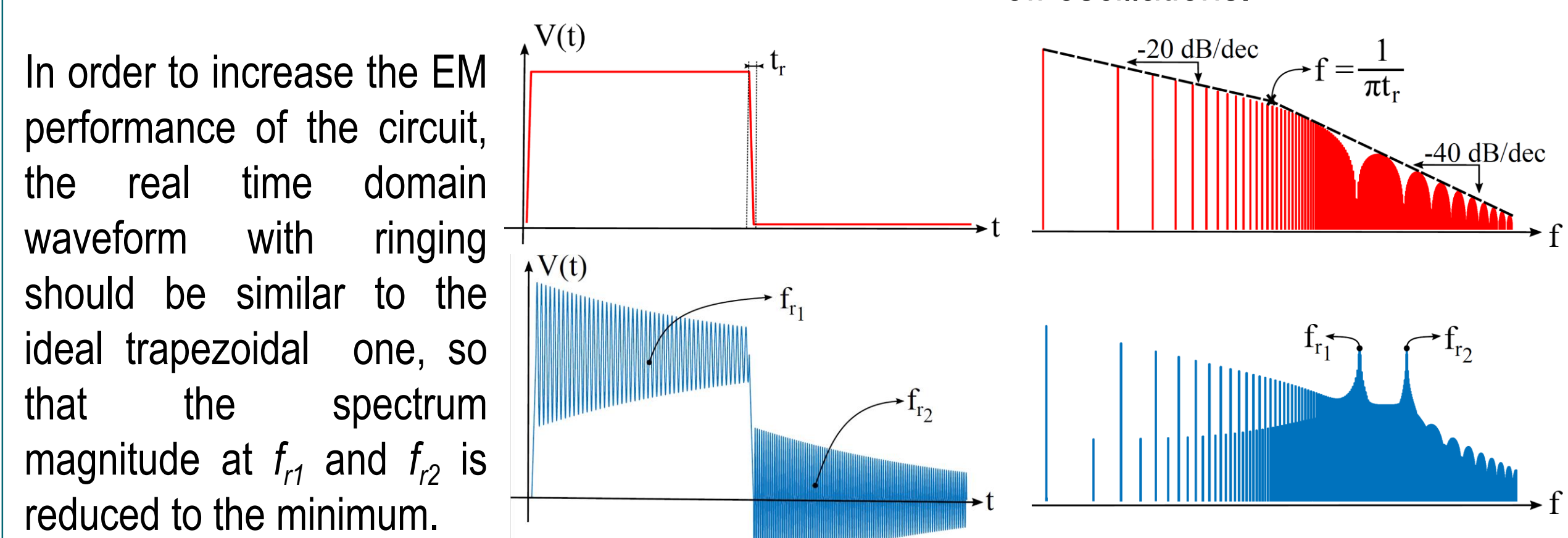
Switching Noise of DC-DC Converters

The generic trapezoidal waveform is of particular interest because it represents the ideal transition shape for voltages and currents in power converters. The frequency spectrum of such waveforms is strictly related to the one of EM emission and for this reason it should be kept under the established limits.



The parasitic elements, included in each power converter, deflect the trapezoidal switching waveforms from the ideal one, causing oscillations and deteriorating its frequency spectrum including two peaks.

The first peak depends on the oscillations caused by the power transistor turn-on, while the second one is related to the turn-off oscillations.



In order to increase the EM performance of the circuit, the real time domain waveform with ringing should be similar to the ideal trapezoidal one, so that the spectrum magnitude at f_{r1} and f_{r2} is reduced to the minimum.

As mentioned before, the most common technique to obtain such a behavior consists of inserting a couple of RC snubbers in parallel to the switching nodes. The values of the snubber components can be evaluated performing the following steps:

- Evaluate the resonance frequency f_r
- Add in parallel to the switching node a known capacitance C_{par} and evaluate the new resonance frequency $f_{r,par}$
- Evaluate the equivalent parasitic capacitance and the equivalent parasitic inductance using the following equations:

$$C_p = \frac{C_{par}}{\left(\frac{f_r}{f_{r,par}}\right)^2 - 1} \quad L_p = \frac{1}{(2\pi f_{res})^2 \cdot C_p}$$

- The optimal values for RC snubbers can be finally derived using:

$$R_{snubber} = 0.65 \sqrt{\frac{L_p}{C_p}} \quad C_{snubber} = 8C_p$$

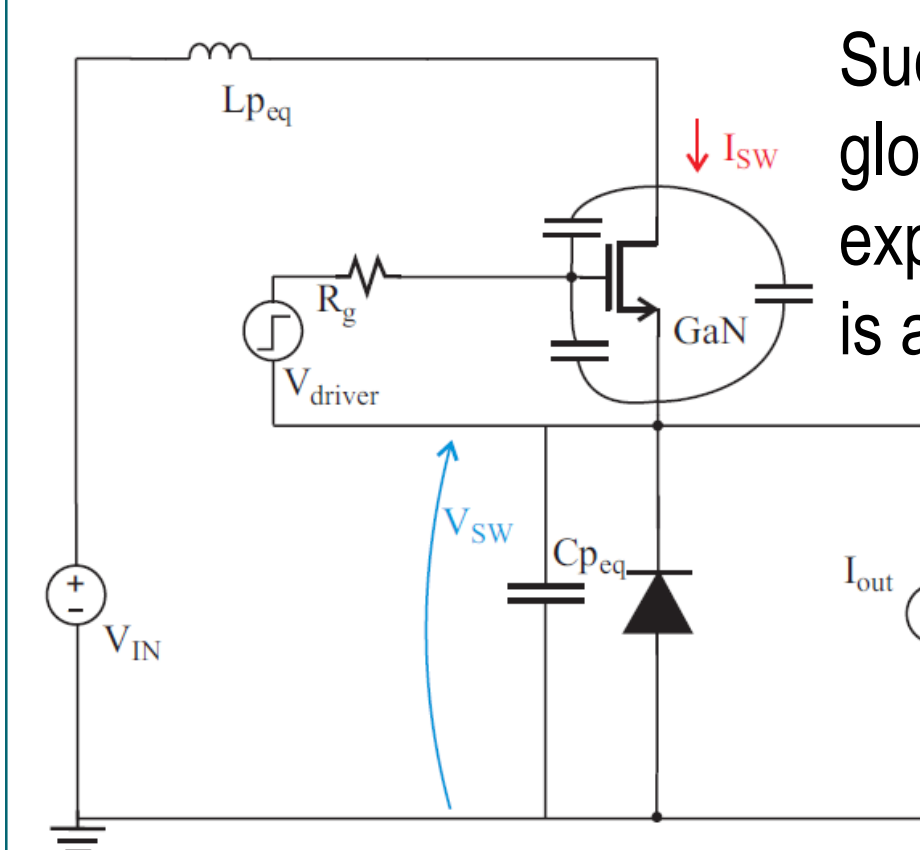
Submitted and published works

- Quitadamo M.V., Raviola, E., Fiori, F., "A Criterion for an Optimal Switching of Power Transistors", 12th International Workshop on Electromagnetic Compatibility of Integrated Circuits, Haining, 2019
- Quitadamo M.V., Raviola, E., Fiori, F., "Investigation on the Switching Waveforms of GaN Power Devices to Gate Current Profiles", International Conference On Power Electronics, Control & Automation, New Delhi, 2019
- Quitadamo, M. V., Fiori, F. "A Spice macro-model for EMC Analysis", Technical Program and Book of Abstracts, Società Italiana di Elettronica (ITALIA) 50TH Annual Meeting of the Associazione Società italiana di Elettronica, Napoli (Italy), 20-22 giugno 2018, pp. 2, 2018, Vol. 1
- Quitadamo, M. V., Fiori, F. "A New Approach to Characterize Complex ICs in Terms of Scattering Parameters", Technical Program and Book of Abstracts, Società Italiana di Elettronica (ITALIA) 49TH Annual Meeting of the Associazione Società italiana di Elettronica, Napoli (Italy), 21-23 giugno 2017, pp. 148-149, 2017, Vol. 1

Adopted methodologies

The evaluation of parasitic elements is the starting point for the implementation of our model.

- An equivalent circuit, modeling the high frequency behavior of the complete buck converter, was designed in order to simplify the analysis.



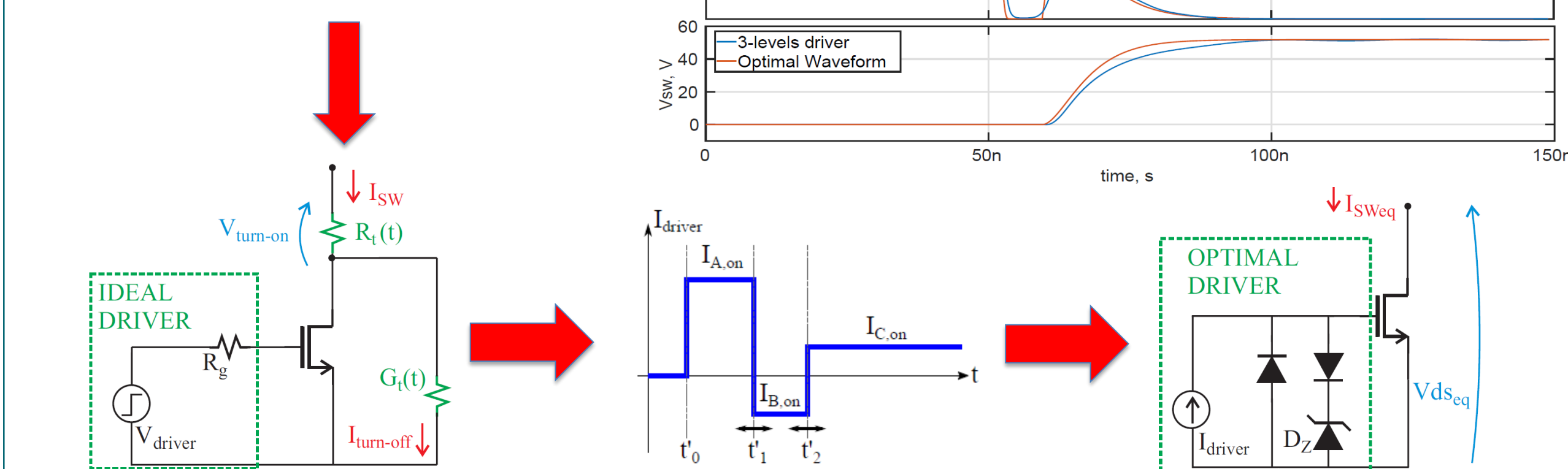
Such circuit includes the GaN model, an ideal diode and two global parasitics, an inductance and a capacitance, evaluated exploiting the procedure used for the snubber design. The load is a constant current source, while the driver is an ideal one.

After the validation of the model, the turn-on and turn-off transitions were analyzed to understand which events cause oscillations and which parasitics are involved in those phenomena. Such analysis highlights that the oscillations, after the turn-on are caused by the voltage

transition and involve C_{peq} and L_{peq} , while the turn-off oscillations are triggered by the current transition and involve L_{peq} and the equivalent parasitic capacitance of the GaN.

- An $R(t)$ and $G(t)$ dissipative elements were defined, the first as function of the derivative of V_{sw} and the second as function of the derivative of I_{sw} . Such elements have been inserted in the converter and the coefficients k_1 and k_2 have been evaluated performing parametric simulations in order to obtain a critically damped system.
- Finally, exploiting Miller's effect, such optimal waveforms were reproduced injecting a 3 constant level piecewise current into the GaN gate. For the turn-on, the first and the third levels were positive and second one was negative, while, for the turn-off, a waveform with dual levels was used.

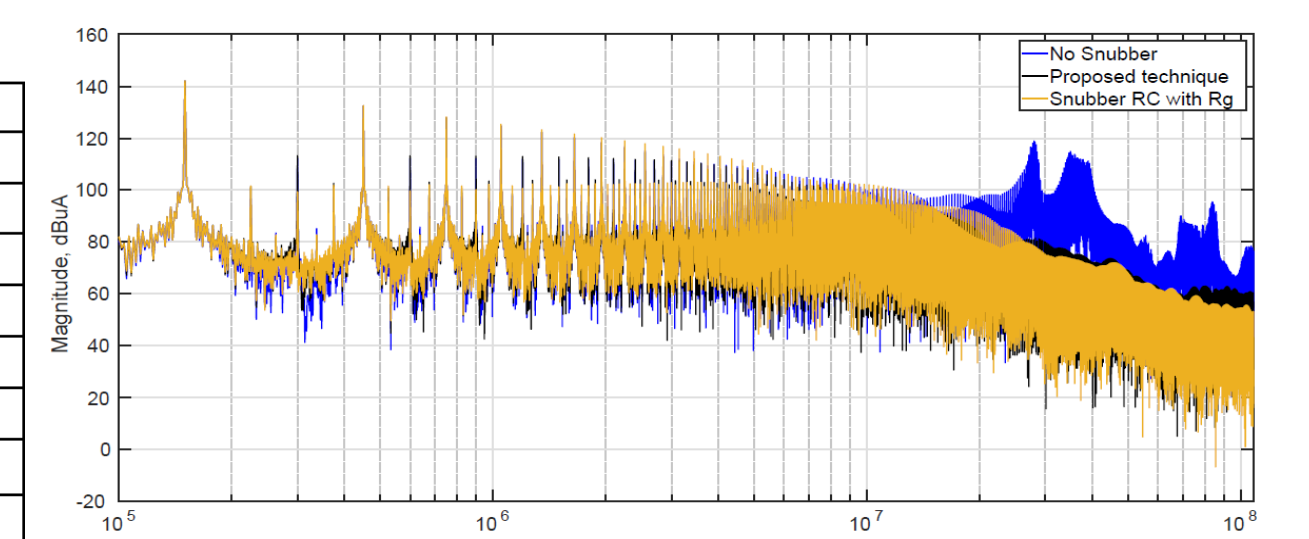
$$R_t(t) = k_1 \frac{dV_{sw}}{dt} \quad G_t(t) = k_2 \frac{dI_{sw}}{dt}$$



Novel contributions

- The developed technique allows to obtain a power saving of about 50% compared to standard solutions, avoiding the use of RC snubbers and the fixed gate resistance.
- The frequency spectrum of the switching current of the active snubbered circuit does not present the peaks due to oscillations

	No Snubber	Snubber RC with Rg	3-level
P_{sw}	1.62 W	4.68 W	3.66 W
P_{diode}	221 mW	198 mW	200 mW
P_{lsnb}	//	1.43 W	//
P_{hsnb}	//	1.26 W	//
P_{tot}	1.84 mW	7.57 W	3.86 W
V_{swp}	103 V	58 V	52 V
V_{dsp}	193 V	65 V	68 V
I_{swp}	33 A	30 A	25 A



Future work

- Investigate the relation between the gate charge, the V_{ds} voltage and the time instants at which the driver current should commute.
- Design and prototype a driver circuit, exploiting the proposed technique.

List of attended classes

- 02LWHRV Communication (15.02.18, 1 credit)
- 01MNFUI Advanced design for signal integrity and compliance (14.09.18, 6 credits)
- 01SFURV Programmazione scientifica avanzata in Matlab (20.04.18, 4 credits)
- 08IXTRV Project Management (12.07.18, 1 credit)
- 01RISRV Public speaking (15.02.18, 1 credit)
- 01SWQRV Responsible research and innovation (13.09.18, 1 credit)
- 02RHORV The new internet society (04.07.18, 1 credit)
- 01SWPRV Time management (06.07.18, 1 credit)
- 01RNBRV Communication II (28.09.2018, 4 credits)
- 01TETRU Forensic Metrology (21.03.2019, 4 credits)
- 01RNCRV Public Speaking II (28.09.2018, 2 credits)
- 01SHFRO Vibration Based Statistical Time Series Methods for Structural Health, (26.10.2018, 2 credits)
- 01LEXRP Strumenti e tecnologie per lo sviluppo del prodotto (12.09.2019, 5 credits)