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XXXIII Cycle

# High resolution DAC based on delta-sigma and DDPM


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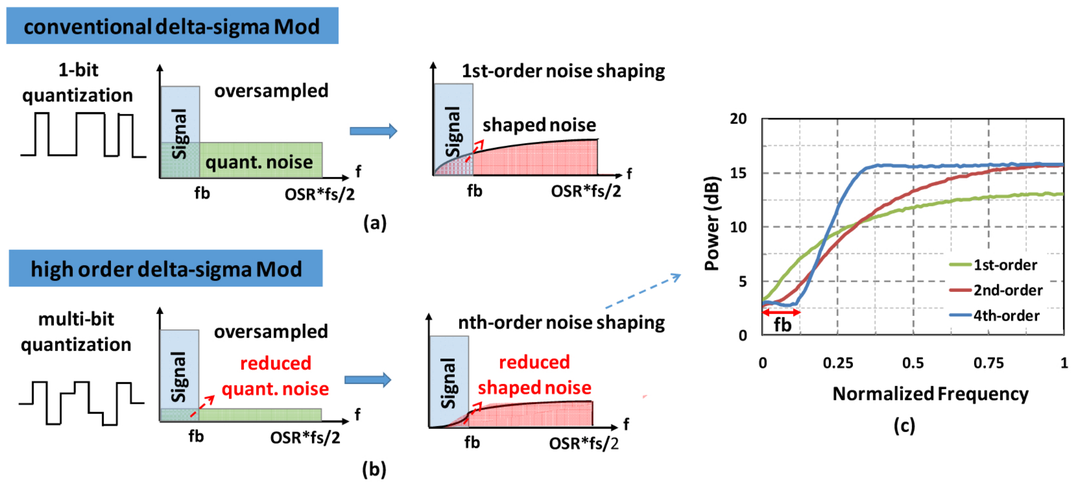
## Research context and motivation

- Many smart signal processing tasks can be carried out in the digital domain thanks to the robustness and reliability of numeric computation but the physical world needs to deal with analog signals, thus the need for high quality Digital-to-Analog Converters (DACs).




- Nowadays it is easy to automate digital circuit designs and make them future-proof thanks to the Moore law of exponentially increasing digital computation power.
- Analog design is more difficult to address, requiring tight tolerances (expensive calibrations and trimming in high end integrated circuits) and high power consumptions to overcome mismatch and noise-related errors. This increase the cost and the reliability of the final device.
- High performance DACs can be used as a building block for high quality Analog-to-Digital Converters (ADCs), assuming that the DAC ensures a good linearity, low noise and low delay.
- High performance DACs and ADCs are often needed in real life applications, leading to mixed-signal integrated circuits which are difficult to design. Hence the need of remaining "as most digital as possible" to be less affected by the analog errors.
- It is possible to trade off amplitude resolution for time resolution, much cheaper in modern integrated circuits, using the Delta-Sigma ($\Delta\Sigma$) modulation technique: the quantization noise is pushed in out of band thanks to a combination of input signal oversampling and quantization noise shaping.
- 1 bit DACs (featuring just two possible levels) are inherently linear while multi-bit (multi-level) DACs are prone to analog errors, in particular static mismatches that generate nonlinear distortions. In return, multi-bit DACs are less sensitive to dynamic errors like clock jitter and inter-symbol interference (ISI).

## Addressed research questions/problems

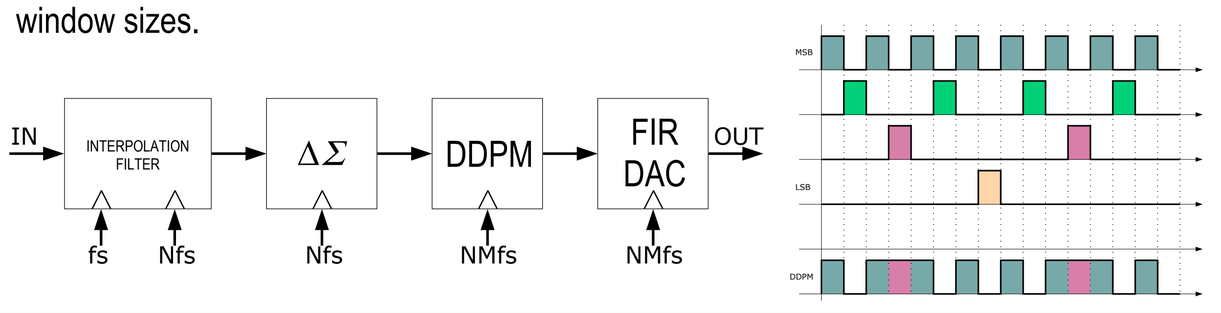
- A linear multi-level DAC is usually achieved with a multi-bit $\Delta\Sigma$ modulator and a Dynamic Element Matching (DEM) scheme. The DEM maps the multi-bit digital word to a finite set of single bit DACs in a thermometer-like fashion but following some constraints in order to tame the mismatch (by ensuring equal utilization of all the single DAC elements) and, in recent works, the ISI by means of complicated digital schemes (by ensuring a more or less constant transition density value for each DAC element).
- The DEM block adds latency, area and power consumption: the DEM, in facts, decomposes the multi-bit signal as a sum of single bits, following a local $\Delta\Sigma$ scheme. The complexity of the DEM grows exponentially with respect to the number of bits required and it is difficult to make high order DEMs.
- It is difficult to design stable single bit $\Delta\Sigma$ modulators with high in-band Signal-to-Quantization Noise Ratio (SQNR). A multi-bit modulator is inherently much more stable and achieves higher SQNR values but it is difficult to replicate the outcome of the digital modulator in the analog domain as each nonlinearity (in particular harmonic distortion) adds up as noise, degrading the Signal to Noise Ratio (SNR).

## Submitted and published works

- Chiara Bartolozzi, Paolo Motto Ros, Riccardo Peloso, Francesco Diotalevi, Marco Crepaldi, Maurizio Martina and Danilo Demarchi; "Live Demonstration: Tactile Events from Off-The-Shelf Sensors in a Robotic Skin", IEEE International Symposium on Circuits and Systems (ISCAS) 2018
- Paolo Selvo, Maurizio Masera, Riccardo Peloso, Guido Masera, Muhammad Shafique and Maurizio Martina; "An Optimized Partial-Distortion-Elimination Based Sum-of-Absolute-Differences Architecture for High-Efficiency-Video-Coding", APPLEPIES 2018
- Paltrinieri Alberto, Peloso Riccardo, Masera Guido, Shafique Muhammad, Martina Maurizio; “Approximate-Computing Architectures for Motion Estimation in HEVC”, New Generation of CAS (NGCAS) 2018
- Capra Maurizio, Peloso Riccardo, Masera Guido, Ruo Roch Massimo, Martina Maurizio; “Edge Computing: A Survey On the Hardware Requirements in the Internet of Things World”, FUTURE INTERNET 2019
- Paltrinieri Alberto, Peloso Riccardo, Masera Guido, Shafique Muhammad, Martina Maurizio; “On the Effect of Approximate-Computing in Motion Estimation”, JOURNAL OF LOW POWER ELECTRONICS 2019

## Novel contributions

- In 2016, professor Paolo Crovetti (POLITO) presented a novel modulation scheme to code a multi-bit word using an oversampled stream of single bits, called Dyadic Digital Pulse Modulation (DDPM), demonstrating that it behaves like a sample and hold in the low frequency region, thus avoiding the distortions typical of PWM modulation while maintaining a very energy-efficient structure.
- His works is being coupled with the $\Delta\Sigma$ approach to reduce the number of bits required to reproduce a high resolution signal, allowing a better spectral utilization. This reduces the required oversampling and thus the total clock frequency, making possible to separate the low oversampling $\Delta\Sigma$ multibit from the high frequency DDPM part.
- The output signal can be filtered using a FIR-DAC approach, which consists on a chain of registers that acts as a moving average filter. This filter presents notches at the frequency of the DDPM peaks, requiring a simpler analog reconstruction filter. It also mitigates the ISI and the jitter sensitivity.
- In order to build the oversampled signal from the Nyquist-sampled input, there is the need of a good interpolation filter. Usually long FIR filters are required to obtain good results and linear phase. A novel hybrid Discrete Sine Transform (DST) and linear interpolation based filter is employed, which adapts to the current sample window to create the missing information. In particular, this new structure decompose the signal in a linear part (the line that connects the two extrema) and the oscillating part, which will start and end with a zero-valued sample. The DST-I is used for trigonometric interpolation of the oscillating part and the result is added to the linear interpolation result, creating a good result even with small window sizes.




## Adopted methodologies

- The $\Delta\Sigma$ loop filter has been designed from scratch resorting to an arbitrary magnitude filter designer in MATLAB. It can design better filters than the one created by using traditional design methods (in primis the $\Delta\Sigma$ toolbox).
- The $\Delta\Sigma$ and the DDPM have been synthesized for an FPGA to assess performances, in part using the MATLAB Simulink HDL coder, and a daughterboard is under development for measuring purposes.
- The hybrid interpolation filter is developed as MATLAB code and it will be implemented on the same FPGA through hardware acceleration.

## Future work

- The performance assessment is under study. In particular there is the need to find the best parameters for the $\Delta\Sigma$ modulator and the number of bits for the DDPM modulator to ensure low power and high performances.
- The hybrid interpolation filter will be better investigated.
- Long FIR filters present better time-domain results but they requires a lot of resources. The state of the art for audio interpolation is the 1M taps filter by Chord Electronics which employs an inefficient traditional filtering on FPGA. A method for long filter design, thanks to Truncated IIR filters (TIIR), is under development for very efficient linear filters. It consists on piecewise exponential approximation of a long low-pass FIR filter by using oscillating low order IIR filters.

## List of attended classes

- 01QTEIU - Data mining concepts and algorithms (6/3/2018, 20 hours)
- 01TEVRV - Deep learning (didattica di eccellenza) (4/6/2019, 30 hours)
- 01LCPIU - Experimental modeling: costruzione di modelli da dati sperimentali (27/9/2018, 33 hours)
- 01SGURV - Intellectual Property Rights, Technology Transfer and Hi-Tech Entrepreneurship (22/3/2018, 30 hours)
- 01MNFIU - Parallel and distributed computing (27/6/2018, 25 hours)
- 01SFURV - Programmazione scientifica avanzata in MATLAB (20/4/2018, 20 hours)
- 01QSCIU - Reconfigurable computing (15/6/2018, 20 hours)
- 01SHCRV - Unsupervised neural networks (didattica di eccellenza) (9/4/2018, 30 hours)
- 01QORRV - Writing Scientific Papers in English (21/3/2018, 15 hours)

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