XXXIII Cycle

CMOS distributed signal processing systems for radiation sensors

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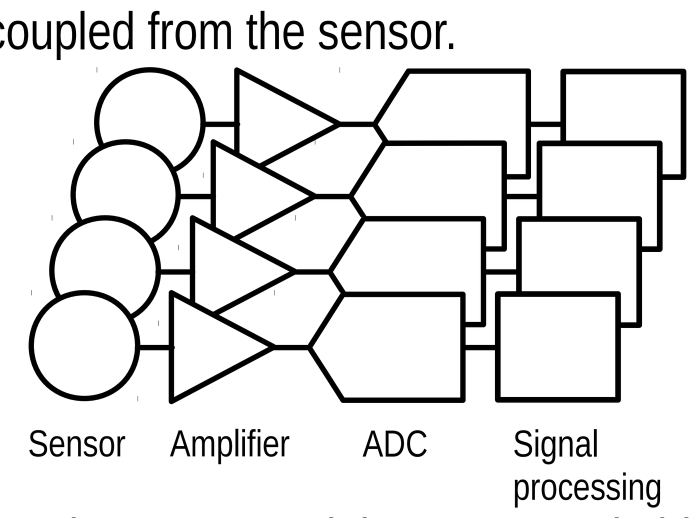
Research context and motivation

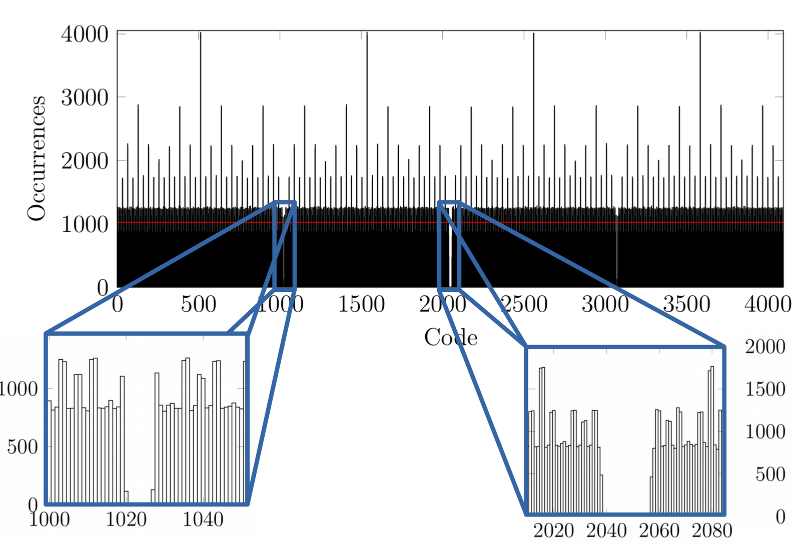
- There are two kind of **radiation detectors** in High Energy Physics (HEP) experiments. In **monolithic** pixel sensors, the electronic shares the same die of the active pixel, while in the **hybrid** solution the implemented electronic is decoupled from the sensor.
- A standard readout system requires **multichannel architecture** (typically 10–100 channels), 8-12 bits of resolution, up to 160 MS/s, low-power consumption and **radiation harness** feature.
- Furthermore, both amplitude and time measurements are required to properly identify the event source.



- These requirements lead to custom solutions rather than commercial ones. A suitable **Digital Signal Processing** (DSP) block completes the acquisition chain.

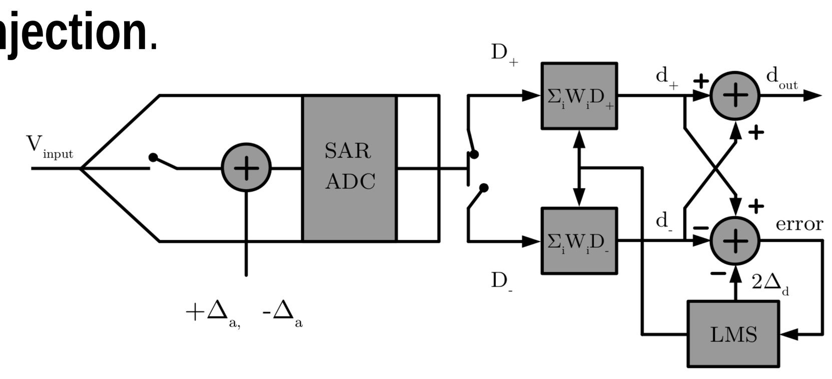
Addressed research questions/problems

- After the acquisition from the sensors, the signal have to be processed by an amplification stage, then it must be digitized through an Analog-to-Digital Converter (ADC).

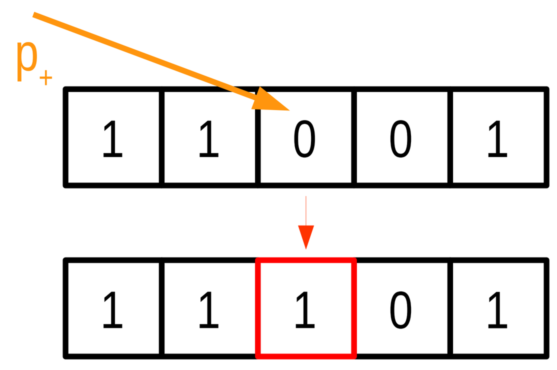


- The explored architecture is a fully differential **Successive Approximation Register** (SAR) ADC. The nominal resolution is **12 bits**. During the conversion process could occur a data loss (**missing codes**) due to the non-linearity of the system.
- In order to solve this lack, it is possible to implement a **calibration circuit** on-chip. The technique adopted for this work is named **Offset Double Conversion** (ODC). It is based on the **superposition principle** and an **offset injection**.

A sample is converted twice. The first time is added the analog offset, in the second one is subtracted the same quantity. Thus, a dedicated circuit provides the double injection.



Taking into account the offset, the subtraction of these two quantities gives an exstimation of the conversion error. This deviation can be corrected using a suitable array of weights.



- Moreover, due to their environment applications, these devices can suffer from a **Single Event Upset** (SEU). Indeed the interaction of a particle could deposit a **local charge** inside the silicon substrate, then a bit-flip can occur in a register.
- The last stage involves a Digital Signal Processing (DSP) block to process the incoming data.

The DSP stage should basically perform a **filter action** to reduce the noise on the sampled data. Depending on the signal shape, a **compression algorithm** could also required. It is also desirable a real-time **spectrum analysis** to perform a Fast Fourier Transform (FFT).

External training activities

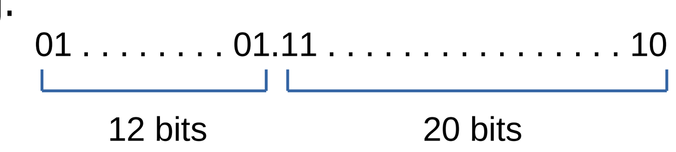
- *XXVII Giornate di studio sui rivelatori - Scuola F. Bonaudi*, Cogne (AO), 12-16 February 2018 (25 h).
- *Efficient Machine Learning for IoT*, EPFL (Switzerland), 23-24 August 2018 (12 h).
- *VIII International Course "Detectors and Electronics for High Energy Physics, Astrophysics, Space Applications and Medical Physics"*, INFN National Laboratories of Legnaro (PD), 1-5 April 2019 (30 h).
- *Essential verification with System Verilog and UVM*, Europractice training course, imec, Leuven (Belgium), 30 September – 4 October 2019.

Submitted and published works

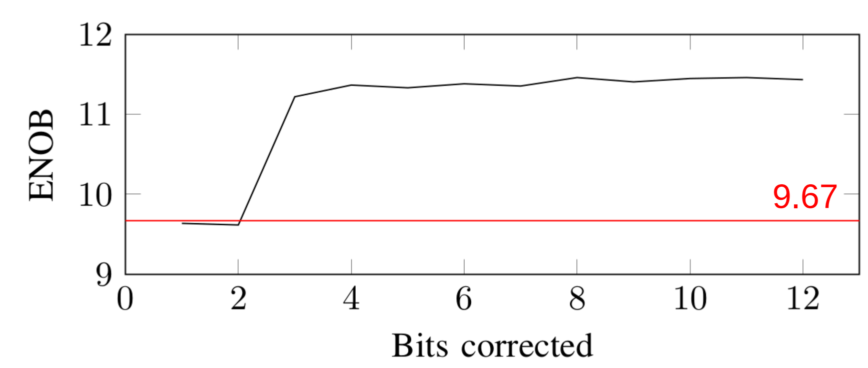
- Ciciriello, F.; Marzocca, C.; Demaria, L.; Pacher, L.; Rotondo, F.; Wheadon, R.; Di Salvo, A.; Mazzucchelli, P., *"A Rad-Hard 12-bit Auto-Calibrated ADC in CMOS 65nm"*, 2017 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), IEEE, 2017.
- G. Baruffa, P. Placidi, A. Di Salvo, S. Marconi and A. Paternò, *"An Improved Algorithm for On-Chip Clustering and Lossless Data Compression of HL-LHC Pixel Hits"*, poster accepted at IEEE 2018 NSS/MIC/RTSD, Sydney, 10–17 November 2018.
- A. Di Salvo, *"Design of a 12-bit SAR ADC with digital self-calibration for radiation detectors front-ends"*, 15th Conference on Ph.D. Research in Microelectronics and Electronics, PRIME 2019, Lausanne (Switzerland), 15-18 July 2019.
- R. A. Giampaolo, A. Di Salvo, L. Pancheri, T. Croci, J. Olave, A. Rivetti, M. Da Rocha Rolo, S. Mattiazzo, P. Giubilato, *"Depleted MAPS on a 110 nm CMOS CIS Technology"*, 26th IEEE International Conference on Electronics Circuits and Systems, Genova, Italy, 27-29 November 2019 [in press].

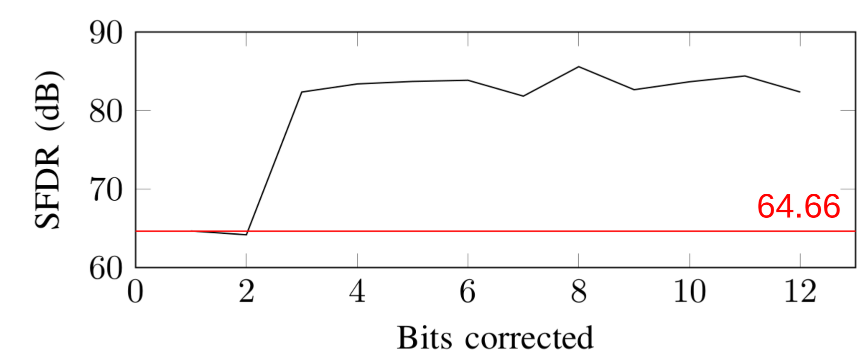
Novel contributions

- A **single-channel prototype** was submitted in **110 nm CMOS** technology with four metal layers available. This run will allow to test both the injection system and the calibration engine.
- The efforts concerned the physical implementation of the algorithm and its integration with the other blocks. The original method was simplify using:



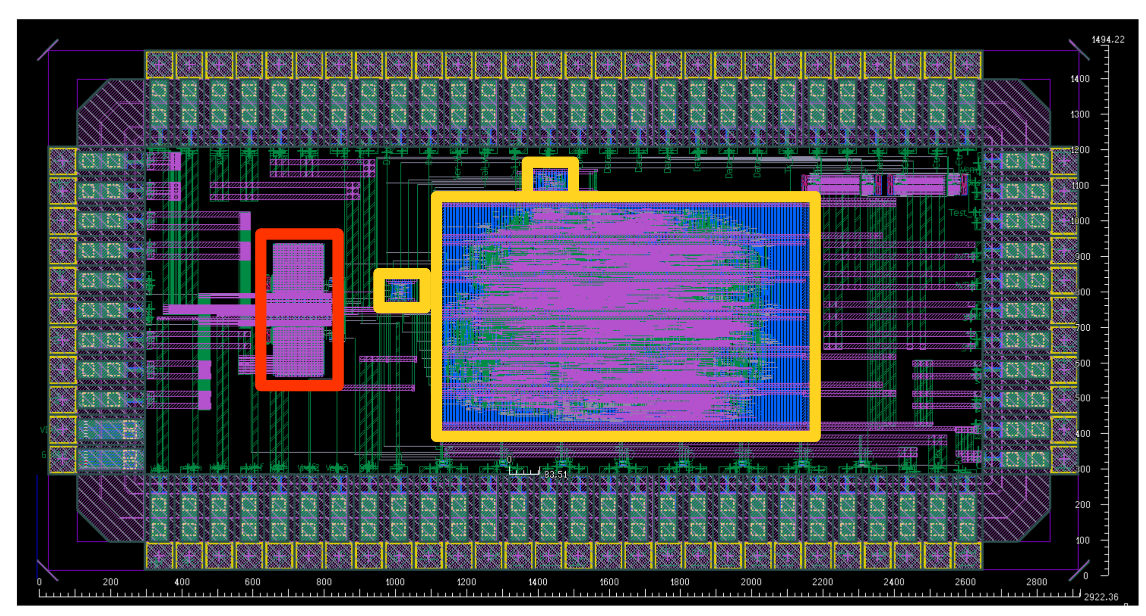
- 32 bit fixed point representation, **Q(12.20)**.
- Programmable learning parameters to adapt the algorithm to different ADC-scenarios.
- Auto-detect function to discriminate the double conversion.





- Furthermore, a study about the **performance** of the algorithm was carried out. This analysis could be useful in a future upgrade of the test-chip to save more area, power and calibration time.

Adopted methodologies



- The yellow boxes highlight the digital domain of the test chip. The smaller boxes are **two serializers** (one of which is configurable), the larger one is the **calibration engine**. Inside the correction block was accomodate a **slow-control** coupled to another dedicated serializer to write and read the most important registers.
- The main efforts has been done for the implementation of the scripts. The synthesis was performed using Design Compiler. IC Compiler II was adopted to complete the Place & Route phase. The funcionality were tested with PrimeTime and Questa.

	Calibration	Raw serializer	Configurable serializer
Clock (ns)	25	5	5
Area (μm²)	664x1064	72x92	72x126
Power (mW)	0.61	0.0086	0.1234

Future work

- **Testing** and **debugging** of the chip (available in December 2019).
- Completing the acquisition chain with the **DSP block**.
- Applying **radiation protection** to the registers.

List of attended classes

- 01SHCRV – Unsupervised neural networks (didattica di eccellenza) (09/04/2018, 6)
- 01QORRV – Writing Scientific Papers in English (21/02/2018, 3)
- 01SFTRV – Fondamenti probabilistici e visione nella robotica di servizio (12/06/2018, 4)
- 01RISRP – Public speaking (31/08/2018, 1)
- 01QEZRV – Sviluppo e gestione di sistemi di acquisizione dati (29/11/2018, 5)
- 01QSCIU – Reconfigurable computing (11/02/2019, 4)
- 02LWHRV – Communication (14/03/2019, 1)
- 01SHMRV – Entrepreneurial Finance (14/03/2019, 1)
- 03QTIIU – Mimetic learning (08/07/2019, 4)
- 03QRHRV – Microelectronics for radiation detection II (03/06/2019, 4)
- 03LCLRV – Epistemologia della macchina (20/06/2019, 4)

POLITECNICO DI TORINO

PhD program in
Electrical, Electronics and Communications Engineering