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XXXIV Cycle

Radiation Tolerant Analog Design for HEP Experiments in advanced technology nodes

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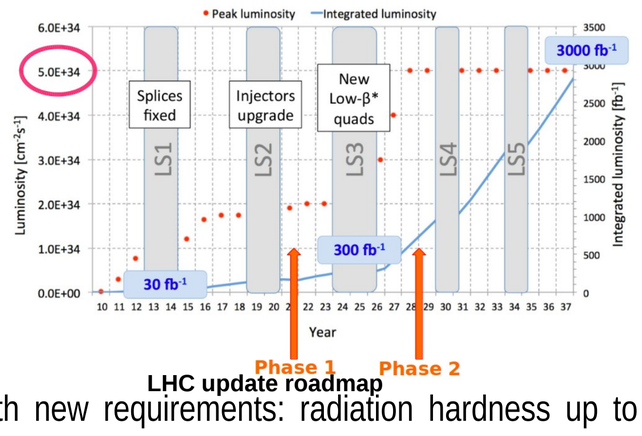
Research context and motivation

- High Energy Physics (HEP) Experiments will enter a new High Luminosity (HL) phase in order to increment statistics of rare events.
- The Large Hadron Collider (LHC) at CERN in Geneva will be upgrade to its HL-phase in 2026, reaching a peak luminosity of $5x10^{34}$ [$cm^{-2}s^{-1}$]
- In this condition detectors electronics must be re-designed in order to cope with new requirements: radiation hardness up to 10^{17}[$n_{eq}cm^{-2}$], data rates of 3 [GHz cm^{-2}] and a number of pile-up events on the order of 200.
- Standard tracking techniques will prove to be inadequate to distinguish single events on the basis of the acquired data.
- The TimeSPOT project by INFN will aim to research and develop a demonstrator of scaled down version of a tracker suitable for HL (comprising the radiation sensor, front-end (FE) electronics, read-out electronics and track-reconstruction electronics.
- In order to properly reconstruct tracks the project will adopt a 4D-Tracking techniques, which requires the particle timing information in addition to the 3D positional one.
- This work is part of the design and realization of the FE electronics for TimeSPOT.



LHC update roadmap

TimeSPOT

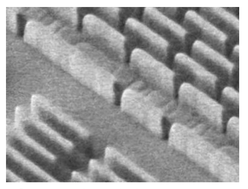
TIME and SPace real-time Operating Tracker

INFN

Istituto Nazionale di Fisica Nucleare

Novel contributions

- Employment of a 28nm CMOS technology, new in the field of radiation tolerant electronics.
- Development of an architecture witch aims to fulfill the requirements of pixel detectors in for HL-HEP experiments:
  - -Pixel pitch of 55x55µm^2.
  - -Timing resolution < 100 ps.
  - -Power consumption of ~40 µW/channel.
  - -Pixel dead time < 1µs in order to sustain 75 KHz per-channel data-rate.
  - -Integration of one TDC per channel
- Usage of a discrete-time technique to compensate per-channel variation and thus avoiding per-pixel calibration.



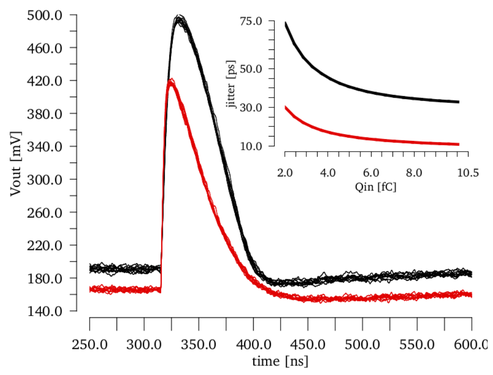
SEM photo CMOS process

Input Signal	Delta-like		Sensor	
Power [µW]	4.1	7.2	4.1	7.2
G [mV fC^{-1}]	190	168	150	124
σ_n [mV]	2.8	2.0	2.8	2.0
ENC [e]	94	77	120	103
t_{pk} [ns]	16.4	7.7	18.2	10.2
t_A [ns]	2.1	2.1	4.2	3.5
TOT [ns]	100	98	79	78
SR [mV ns^{-1}]	53	98	39	68
σ_j [ps]	54	21	74	30
σ_p [ps]	66	65	67	66
σ_{mm} [ps]	33	26	40	29

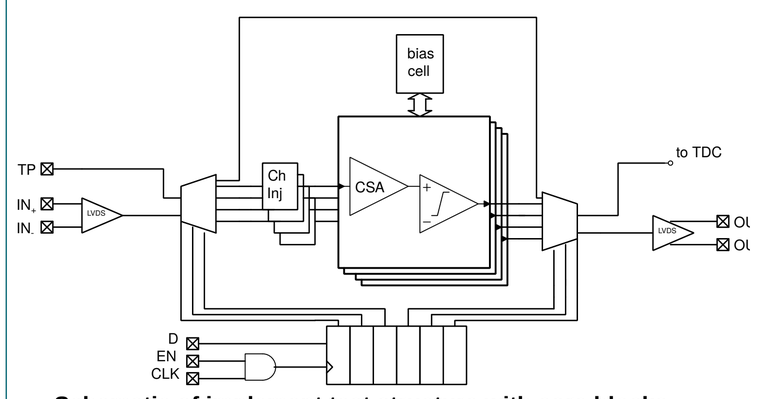
Simulated expected FE performances

Adopted methodologies

- Circuit design and simulation carried out using industry standard EDA tools and CAD.
- Conjoint development and optimization of FE electronics and silicon sensor (impedance matching and signal characteristics).
- Montecarlo simulations for per chip-and per pixel variation due to process and mismatch variations.
- FPGA-based experimental setup for precise and fast control of compensation phase, system pulsing and analog reference setup.



Simulated CSA signal



Schematic of implement test structure with core blocks (repeated in 8 parallel channels)

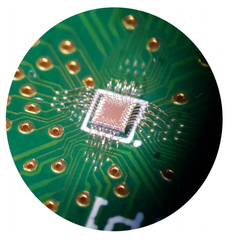
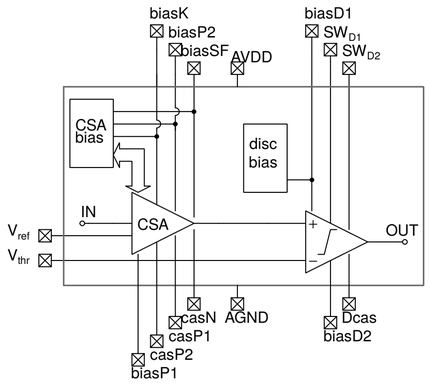
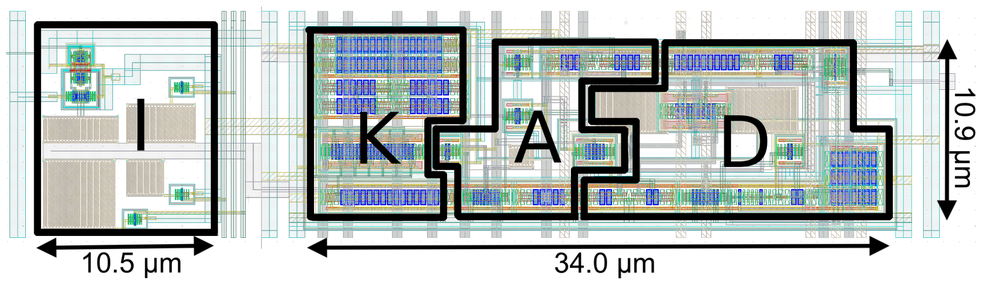


Photo of the first test chip wire bonded to its test board. Now under test



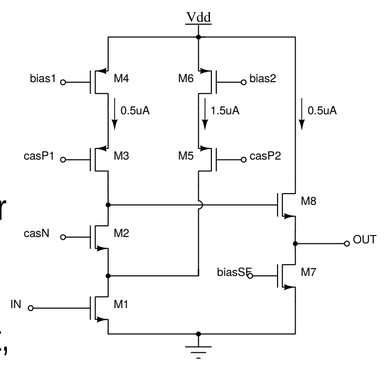
Detailed schematic of th system with essential external references

Addressed research questions/problems



Analog FE full chain Layout

- High granularity timing pixel FE requires a low noise, small area, PVT resistant and high speed design design.
- FE architecture designed with total power budget <10 µW. Composed by:
  - -Core Amplifier (A) : Telescopic Cascode Amplifier with split bias current branches, with toal power consumptio <3µW
  - -Charge Sensitive Amplifier CSA with active feed-back networ (K) with DC leakage current compensation based on Krummenache Filter, with power <100nW and ENC < 100e$^-$.
  - -Leading Edge Discriminator (D) with Offset Correction circuit, PVT aware design with power < 3µW.
  - -Charge Injection Circuit (I) with variable capacitive load for sensor emulation and calibration.
- Necessity to characterize a fast and low-power system: digital IO to overcome band-width limitation: first prototype testable both independently and with the on-chip TDC.



(A)

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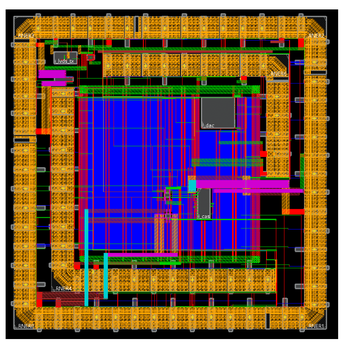
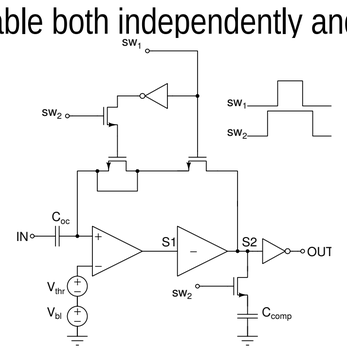
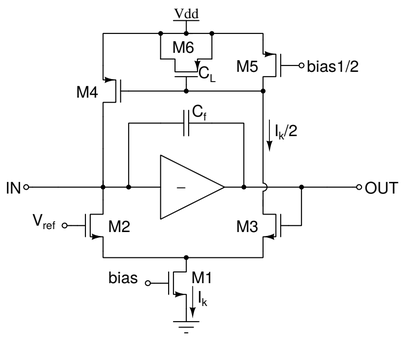


Full Chip Layout of the first prototype



(D)



(K)

Future work

- Ongoing tests on first prototype, which aims to obtain a complete operation and performance characterization.
- Radiation damage tests on first prototype.
- Design of an integrated-on pixel time-walk correction based on Constant Fraction Discriminator (CFD) of Time over Threshold (ToT) measurement.
- Realization of a second prototype chip with the full FE pixel chain organized in a pixel matrix with service blocks and digital I/O. This chip will be coupled via bump-bonding with now-under-test sensor. The second design will be submitted on 4/2020.

Submitted and published works

Lorenzo Piccolo , "*A Timing Pixel Front-End Design for HEP Experiments in 28 nm CMOS Technology*", 2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)

List of attended classes

- 01CLPRV – Experimental modeling (10/2018, 6)
- 01RONKG – Python in the Lab (2/2019, 4)
- 03QRHRV – Microelectronics for radiation detection II (6/2019, 4)
- 02LWHRV – Communication (8/2019, 1)
- 01SHMRV – Entrepreneural Finance (8/2019, 1)
- VIII International Course " Detectors and Electronics for High Energy Physics Atrophysics, Space and Medical Applications" (2/2019, external activity ,30h)

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