ScuDo

Scuola di Dottorato ~ Doctoral School

WHAT YOU ARE,TAKES YOU FAR

XXXIV Cycle

SoC integration for design automation and monitoring in power electronics

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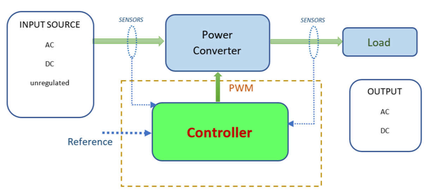
Research context and motivation

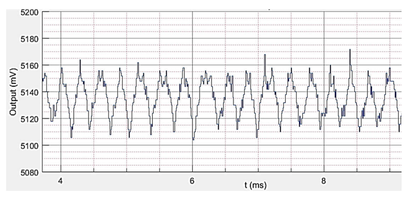
- Digital control systems allow the implementation of complex control strategies with math-intensive and highly parallel algorithms. Advantages of the digital process in power electronics also include low power consumption and lower sensitivity to parameter variations. However, high-performance digital devices are needed for some algorithms to operate in fully digital mode due to very short control interval of switch mode converters, putting analog controllers still as the reference in terms of rapidity and bandwidth. On the other hand, design and monitoring of highly parallel operations in digital control feedback loops are not a trivial task.

- With the advent of system on chip (SoC) devices, and their increasing affordability, abovementioned challenges are facilitated. SoCs feature both FPGA and Hard CPU units in one package, with built-in, very efficient, high speed interfaces. So, it is possible to partition tasks accordingly. Specifically, monitoring parallel operations that run inside FPGA can be easily done through embedded user program running inside CPU unit, which allows to analyze and test the innovative digital control laws for power converters more efficiently and with great details. This also enables to programmatically verify any new control algorithm for all operating conditions, looking for any possible glitches or non-linearities, facilitating the mitigation of such issues.

Addressed research questions/problems

- Investigation of **non-linearities** in switch mode DC-DC converter control using SoC.
- Real-time monitoring of digital feedback loop operation synchronously reading parallel states of the controller for DC-DC converter.
- **Framework for automatic testing** for all different input and load conditions, detection for any possible non-linearities or faults.





- One of the problems which arise in these digitally controlled systems is the presence of non-linear effects, such as Limit Cycle Oscillation (LCO), that can potentially degrade the output voltage regulation of the power electronic systems. These LCOs occur manly due the quantization process which is inherent in the operation of the ADC and the pulse-width-modulator (PWM) within the feedback loop.

Novel contributions

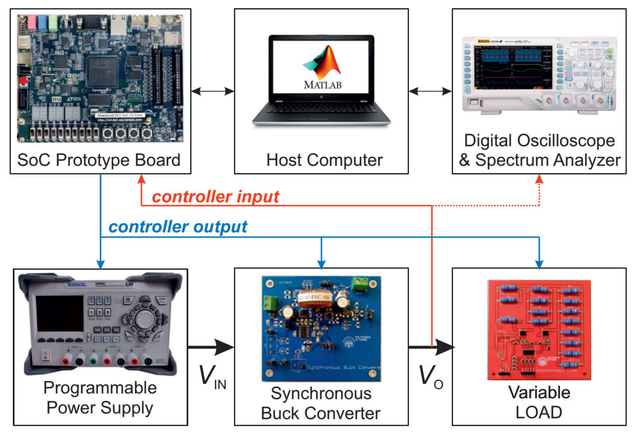
- Framework of real-time monitoring for digital controller prototypes has been designed and SoC-FPGA based solution has been implemented as part of the research activity.
- Developed system has been tested extensively to investigate the problem of Limit-cycle oscillation (LCO) in digitally controlled synchronous buck converters.
- Efficient suppression method of LCO has been achieved utilizing novel Dyadic modulation technique.
- Realization of SoC based monitoring system that had greatly facilitated to make automated experiments with varying parameters and faster data acquisition, allowing to monitor more complex control experiments of different power converter topologies with less effort.

Submitted and published works

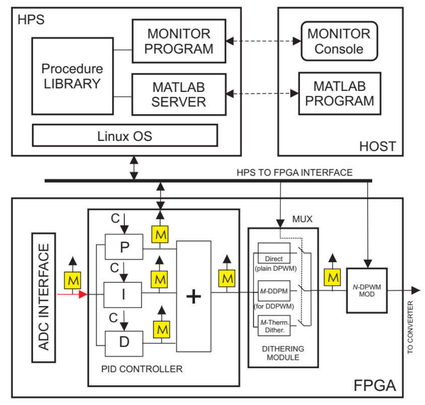
- Maqsudjon Usmonov, Paolo S. Crovetti, Francesco Gregoretti and Francesco Musolino, "*Suppression of Quantization-Induced Limit Cycles in Digitally Controlled DC-DC Converters by Dyadic Digital Pulse Width Modulation*", 2019 IEEE ECCE conference, Baltimore, USA, 2019

Adopted methodologies

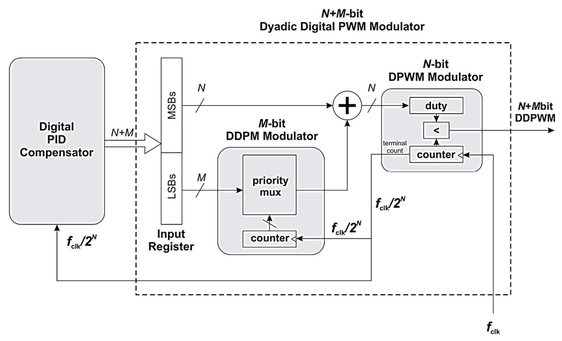
➢ Testbench setup design for experimentation



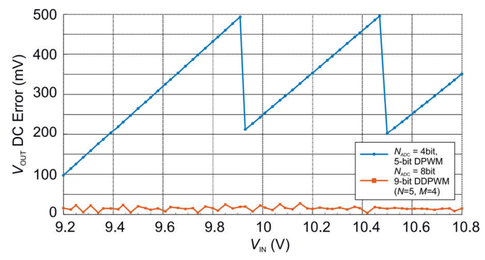
Implementation blocks



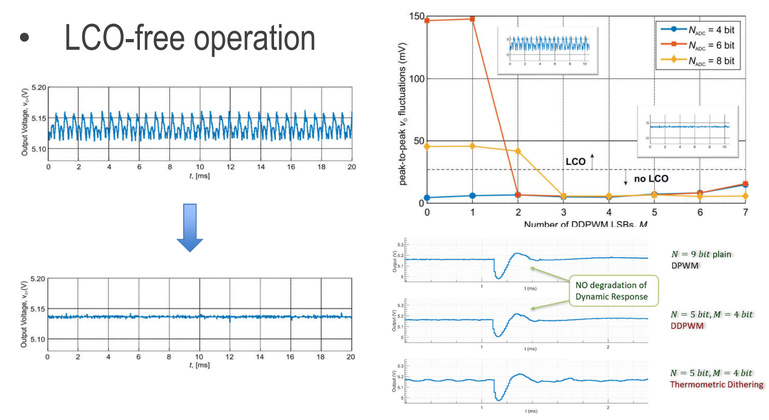
➢ Architecture of Dyadic Digital Pulse Width Modulation



- Automatic testing for different input voltages



- LCO-free operation



Future work

- Further development of the framework to synthesize digital control modules at a higher level, in order to speed up testing procedures of power converter control loop with SoCs and to enable real-time monitoring at comparatively low-cost.
- Feasibility study of applying real-time monitoring to predict component failures of power converters in advance.

List of attended classes

- 01TBXRV – Vision fundamentals in service robotics (23/05/2019, 4 CFU)
- 03QRHRV – Microelectronics for radiation detection II (03/06/2019, 4 CFU)
- 01QORRV – Writing Scientific Papers in English (06/06/2019, 3 CFU)
- 01RONKG - Python in the Lab (25.06.2019, 4 CFU)
- 01TCTRV – Photonext: Hands on course on Photonics for Fiber Transmission (18/07/2019 , 6 CFU)
- 01QFDRV - Photonics: a key enabling technology for engineering applications (12.07.2019, 5 CFU)
- 01LGSRV - Characterization and planning of small-scale multigeneration systems (13.09.2019, 5 CFU)
- 02ITTRV - Generatori e impianti fotovoltaici (26.09.2019, 5 CFU)

External activities:

- 2nd Design Automation for Power electronics (DAPE) Workshop, Genova, (06.09.2019)

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