ScuDo

Scuola di Dottorato ~ Doctoral School

WHAT YOU ARE,TAKES YOU FAR

XXXIV Cycle

Nanoscale CMOS Digital-Based Analog Processing for IoT Applications

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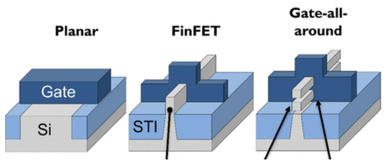
Research context and motivation

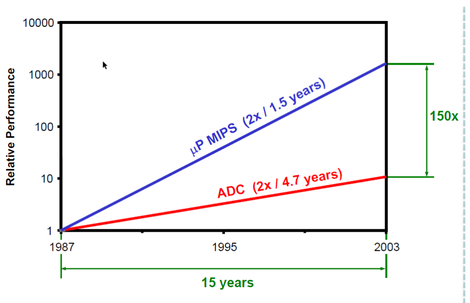
- **IoT Application and Low Power requirement :**

(Source: McKinsey Global Institute.)

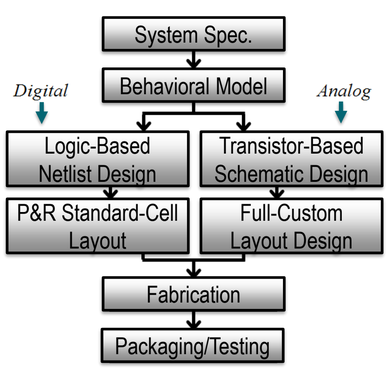
- Ultra Low Power (ULP) systems disruptive IoT applications: logistics, navigation, health and fitness.
- Expected market share of **$2.5 trillion** at 2025.
- **CMOS** is **the IoT technology**.
- **ULP CMOS analog interfaces** always are needed.



- **Analog Design vs Technology vs Design Flow:**



(Comparison performance btw CMOS Digital and Analog system over time. - B. Murmann .: Digitally Assisted Analog Circuits, 2006)

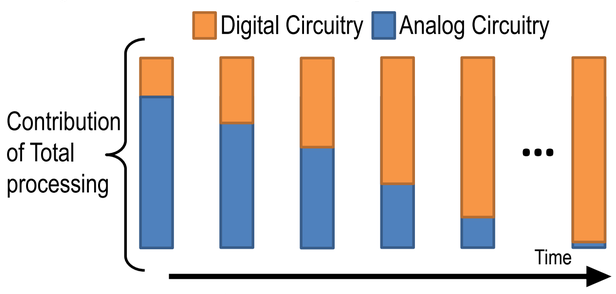


Analog Design Flow:
- Longest design time
- Manual layout
- Labor intensive
- Highest performance

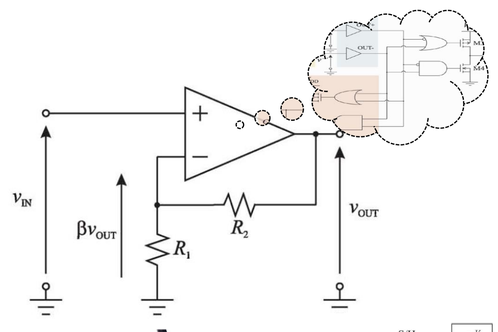
Digital Design Flow:
- Automatic
- Portability
- Time-to-market
- Reasonable performance

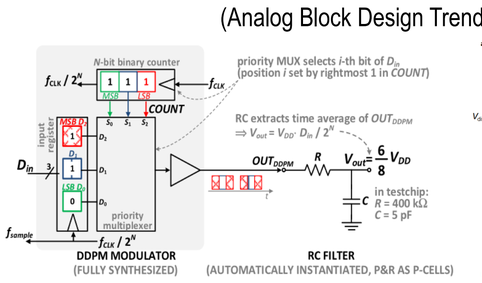
Addressed research questions/problems

- **Increasing trend** in finding alternative IC design strategies **to implement analog functions exploiting digital-in-concept design methodologies**.
- Below **digital-in-concept design trend** and **digital-based analog building blocks done by our Research Group:**

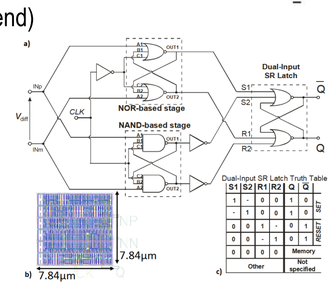


(Analog Block Design Trend)

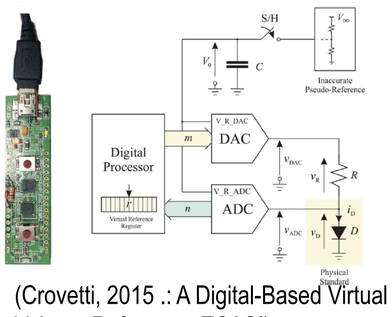




(Aiello,2019, et al.: Fully Synthesizable Low-Area DAC, TCASI)



(Aiello, 2018, et al.: Fully Synthesizable 0.3V Comparator, ISCAS)



(Crovetti, 2015 .: A Digital-Based Virtual Voltage Reference, TCASI)

Novel contributions

- Ultra Low Voltage (ULV) design investigation through the implementation of **a 0.3-1.2V Schottky-Based CMOS ZTC Voltage Reference.**
- **A novel 300 mV Digital-Based Operational Transconductance Amplifier (DB-OTA)**
- The DB-OTA **maximum energy-efficient point** is demonstrated as well as its **scalability**.

Research Collaborations

UFRGS UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL + POLITECNICO DI TORINO + NUS National University of Singapore

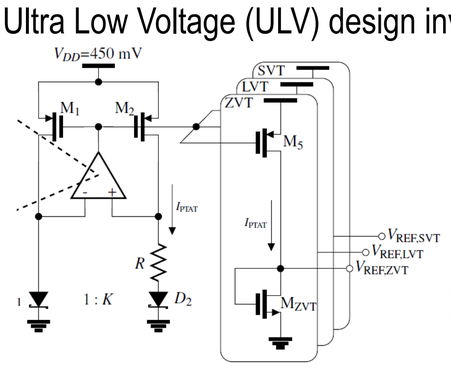
Joint Degree PhD

Submitted and published works

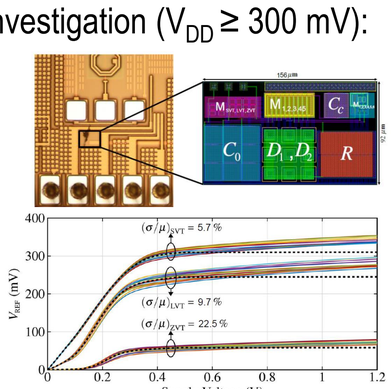
- T. Bradde, P. Toledo, M. Stefano, S. Grivet-Talocia, P. S. Crovetti. “Enabling fast power integrity transient analysis through parameterized small-signal macromodels,” EMC Europe 2019, Barcelona, 2019. (Accepted)
- P. S. Crovetti, F. Musolino, O. Aiello, P. Toledo and R. Rubino, "breaking the boundaries between analogue and digital,“ Electronics Letters, vol. 55, no. 12, pp. 672-673, 13 6 2019.
- P. Toledo, D. Cordova, H. Klimach, S. Bampi and P. Crovetti, "A 0.3-1.2V Schottky-Based CMOS ZTC Voltage Reference," in IEEE Transactions on Circuits and Systems II: Express Briefs., 2019
- P. Toledo, P. Crovetti, H. Klimach and S. Bampi, “A 300mV-Supply, 2nW-Power, 80pF-Load CMOS Digital-Based OTA for IoT Interfaces”, IEEE International Conference on Electronics Circuits and Systems, Genova, 2019 (Accepted)
- P. Toledo, O. Aiello, P. Crovetti “A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration”, IEEE Nordic Circuits and Systems Conference, Helsinki, 2019 (sent)

Adopted methodologies

- Ultra Low Voltage (ULV) design investigation ($V_{DD} \geq 300$ mV):



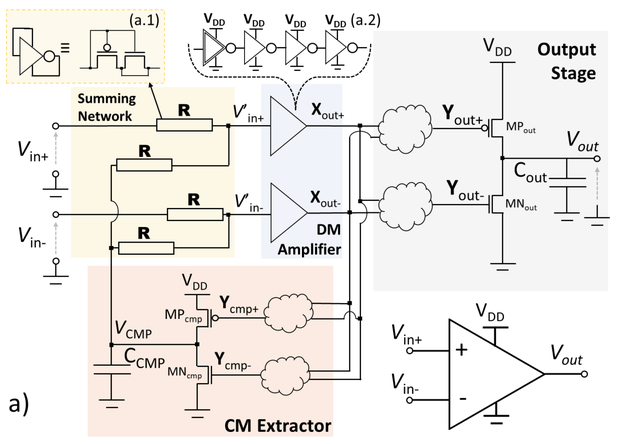
(A 0.3-1.2V Schottky-Based CMOS ZTC Voltage Reference)



(V_{REFs} vs V_{DD}: measurements)

Achievements:
- A 300mV voltage reference circuit operated under the MOSFET ZTC condition.
- Measurements Results.
- 10xless power than previous Schottky-based implementations.

- The proposed ULV DB-OTA has been designed in 180nm following digital design criteria



(ULV DB-OTA circuit schematic)

DM Amplifier

X_{out+}	X_{out-}	X_{out+}	X_{out-}	X_{out+}	X_{out-}	X_{out+}	X_{out-}
1	1	0	0	1	0	0	1

V_{in+} V_{in-} V_T

$V_{CM} > V_T$ $V_{CM} < V_T$ $V_D > 0$ $V_D < 0$ (b.1)

Output Stage

X_{out+}	X_{out-}	Y_{out+}	Y_{out-}
0	0	1	0
0	1	1	1
1	0	0	0
1	1	1	0

$Y_{out+} = \overline{X_{out+} \cdot X_{out-}}$

$Y_{out-} = X_{out-} \cdot \overline{X_{out+}}$ (b.3)

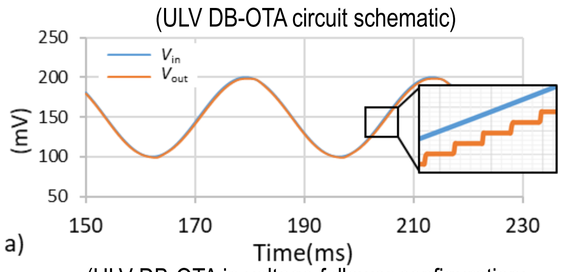
CM Extractor

X_{out+}	X_{out-}	Y_{cmp+}	Y_{cmp-}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

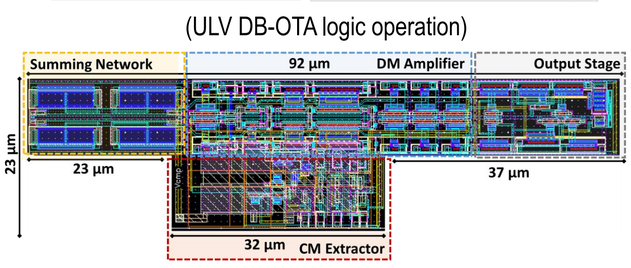
$Y_{cmp+} = X_{out+} + X_{out-}$

$Y_{cmp-} = X_{out+} \cdot X_{out-}$ (b.2)

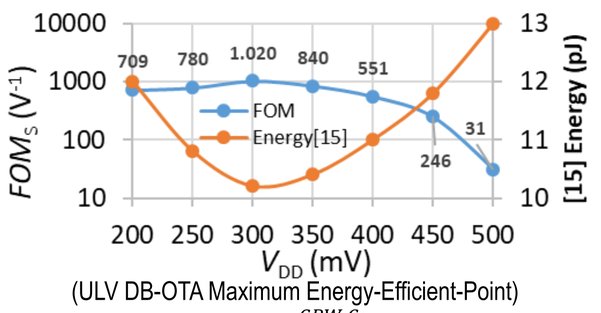
(ULV DB-OTA logic operation)



(ULV DB-OTA in voltage follower configuration: Input and output time domain waveforms)

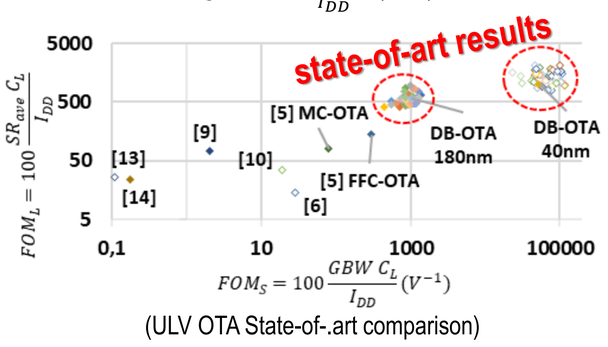


(ULV DB-OTA Standard-Cell-Based layout)



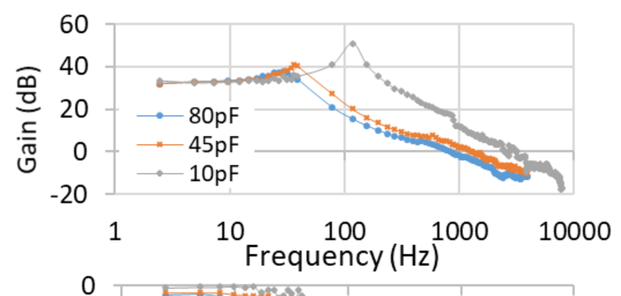
(ULV DB-OTA Maximum Energy-Efficient-Point)

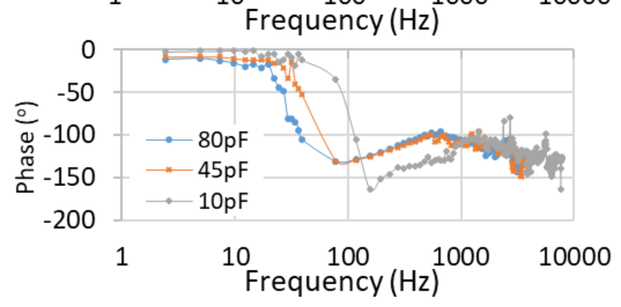
$$FOM_S = 100 \frac{GBW\ C_L}{I_{DD}} (V^{-1})$$



(ULV OTA State-of-.art comparison)

- [5] Lv, L., JSSC, 2019
- [6] Ferreira, L.,TCASI, 2014
- [9] Veldandi, H.,CSSP, 2018
- [10] Abdelfattah,O., TCASI, 2015
- [13] Chatterjee, S, JSSC, 2005
- [14] Ferreira, L. TCASII, 2007





(ULV DB-OTA Frequency response)

- V_{DD} = 300 mV
- Power = 2 nW
- C_{out} = 80 pF
- GBW = 850 Hz
- SR = 0.5 V/ms
- THD = 3%
- $Gain_{DC}$ = 35 dB
- PM = 76 º

Future work

- Development of a ULV DB-OTA compact model.
- Tapeout bring-up is scheduled to the end of 2019.
- Several circuit versions are going to be taped out.
- Development of an automatic measurement testbenchs and the test plan.
- Elaboration of IoT system application with ULV DB-OTA embedded.

List of attended classes

- 02LWHRV – Communication (13/08/2019, 1 CFU)
- 01QRQRV – Compressed sensing: theory and applications (30/05/2019, 4 CFU)
- 01NDLRV – Lingua italiana I livello (12/06/2019, 3 CFU)
- 01SFURV – Programmazione scientifica avanzata in matlab (27/06/2019, 4 CFU)
- 01RISRV – Public speaking (15/08/2019, 1 CFU)
- 01SWQRV – Responsible research and innovation, the impact on social challenges (05/08/2019, 1 CFU)
- 01TCORV – Surrogate and compact modeling: theory for the user (03/09/2019, 4 CFU)

POLITECNICO DI TORINO

PhD program in

Electrical, Electronics and Communications Engineering