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Embedded data converters and front-end for SiPMs in space applications

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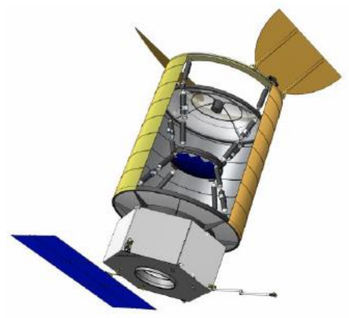
Research context and motivation

- Silicon Photomultipliers (SiPMs) are solid-state detectors composed of a matrix of self-quenched, single-photon avalanche photodiodes (SPADs). The SPADs are designed to work in Geiger mode reverse-biased condition.
- Thanks to their fast response, SiPMs are employed for timing measurement such as in PET or SPECT applications. Moreover, they provides high gain, low operation voltage, compactness and robustness. For these reasons, SiPMs are challenging Photo-Multiplier Tubes (PMTs) in High Energy Physics (HEP) and space experiments.
- This work describes the design of a 64-channel ASIC planned to be used in a satellite application to detect Cherenkov light generated by impinging cosmic neutrinos with the molecules of the Earth atmosphere.
- The ASIC has been designed for the NUSES space mission which will be a path-finder for future missions like POEMMA. The work is carried out within the VLSI Group at INFN.



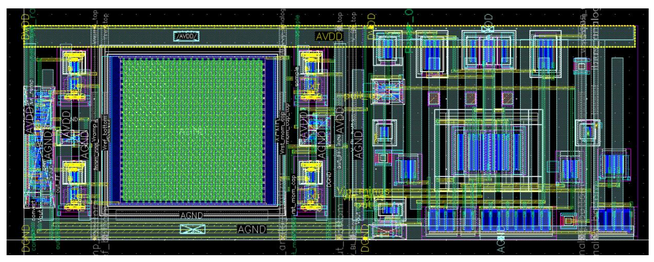
Angela V. Olinto, *POEMMA and EUSO-SPB: Space Probes of the Highest Energy Particles*, 2018

Addressed research questions/problems

- The aim of the experiment is to capture snapshots of few hundreds of nanoseconds after the trigger signal. Hence, a sampling frequency of at least 200 MS/s is needed. Moreover, a high resolution (12 bits) is required.
- Since the ASIC will be employed in space environment, high radiation tolerance is mandatory.
- The power consumption must be kept as low as possibile (target power consumption: ~ 5 mW/ch), so the waveform sampling technique with embedded low-power ADCs is prefeable to the use of free running ADCs placed after the front-end. Hence, each channel includes an analog memory with embedded ADCs which is used to store the input signal with a 5 ns clock.

Adopted methodologies

- The ASIC has been implemented in a 65-nm CMOS technology and operates with a 200 MHz clock frequency and 1.2 V power supply.
- The signal coming from the sensor is amplified and converted into a voltage by an input amplifier. Then, the resulting voltage is buffered into a 256-cells analog memory. If an interesting event is collected, the sampled values are digitized and sent off-chip in Double Data Rate (DDR) differential links. Otherwise, the cells are overwritten. The operation modes of the cells are managed by a digital channel controller.
- The ASIC has been designed and simulated by using professional EDA tools (Cadence).

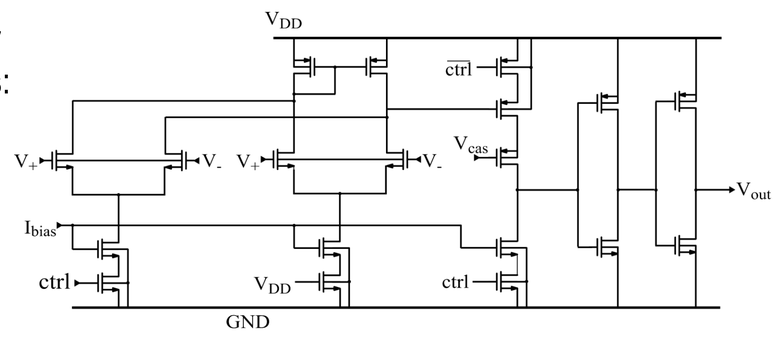


List of attended classes

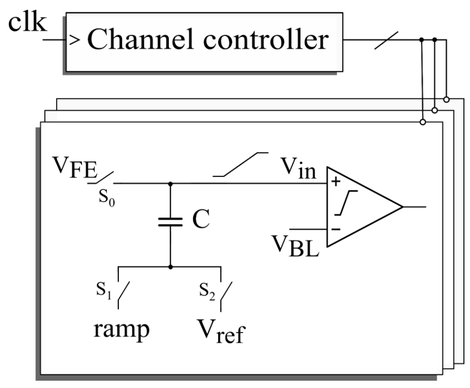
- 01UKAIU – Advanced techniques for digital testing(4/2020, 4)
- 01SIHRV – Bio-Nano Electronics and BioMolecular Computing(7/2020, 4)
- 01UJTIU – Control and data acquisition automation in scientific experiments (1/2020, 2)
- 01QTEIU – Data mining concepts and algorithms (1/2020, 4)
- 02LCPRV – Experimental Modeling (2/2021, 6)
- 01UIXRV – Laboratory of wireless power transfer for electric vehicles (1/2020, 3)
- 04QRHRV – Microelectronics for radiation detection II (9/2021, 4)
- 01UNVRV – Navigating the hiring process: CV, tests, interview (11/2020, 11)
- 01LEVRV – Power system economics (5/2020, 3)
- 01LEVRV – Project management (12/2019, 1)
- 01QEZRV – Sviluppo e gestione di sistemi di acquisizione dati (11/2020, 4)
- 01SWPRV – Time Management (11/2019, 1)
- 01QORRV – Writing Scientific Papers in English (3/2020, 3)
- Introduction to FPGA programming using Xilinx Vivado and VHDL (11/2020)
- Introduction to Analogue ID Design, Simulation, Layout and Verification (12/2020)

Novel contributions

- Each memory cell includes a dedicated 12-bit single-slope ADC composed by a comparator and latches to store the conversion value. The channel embeds a single Gray counter whose outputs are shared among the cells.
- The ramp generator is connected to the bottom plate of the sampling capacitor: during digitization, the top plate is connected only to a gate of a MOS transistor, hence behaves like a floating node. For this reason, the ramp applied to the bottom plate is replicated on the top.
- A single ramp-generator is used for all the cells in a channel to avoid gain non -uniformity. Moreover, the comparator flips always at the same point thus avoiding errors due to common mode variation.
- The comparator of the converter can work in two operation modes:
  - Power-up: during digitization the full bias current (2 µA) is provided to the circuit;
  - Power-down: when the digitization is disabled, the bias current is reduced by a factor 4.

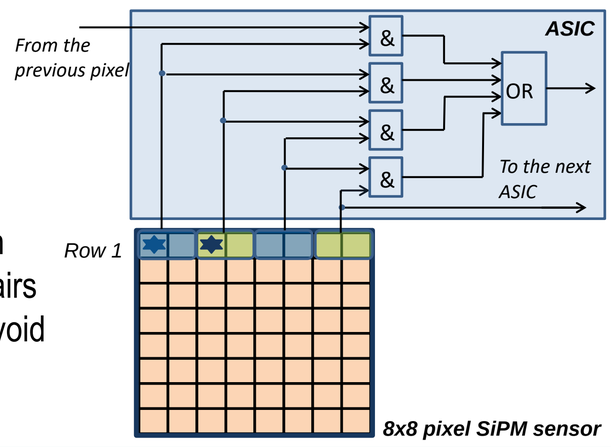


- The memory cells are digitized in parallel thus reducing the conversion time. This dead-time depends on the resolution selected for the ADC which can be tuned between 7 and 12 bits. The dead-time can be halved by counting on both clock edges.
- The analog memory can be further partitioned into 32-cells units (sections). The configuration can be programmed to use segments of 32, 64 or 256 cells. This features reduces the probability of loosing an event because the channel is processing the previous one.
- Moreover, the channels can work in parallel (imaging mode) or independently (sparse mode). This makes the chip more flexible.

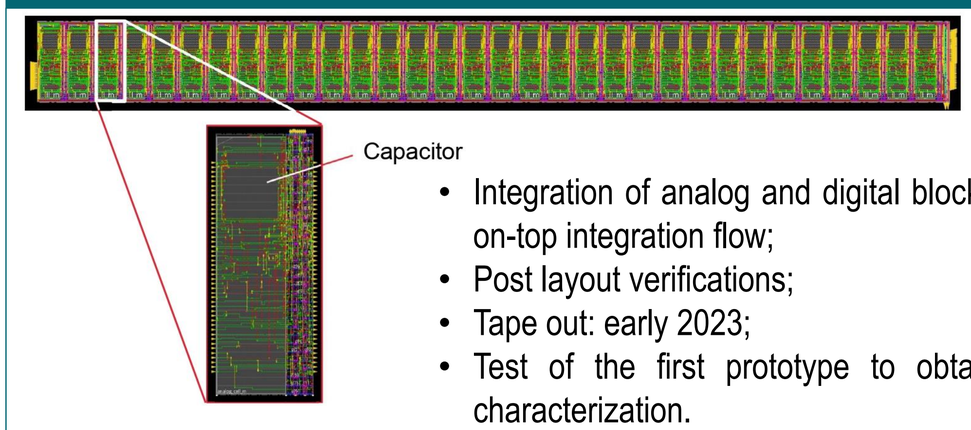


Resolution	ADC conversion time
8 bit	**1.28 µs**
10 bit	**5.12 µs**
12 bit	**20.48 µs**

- The incoming signal is focused on two corresponding pixels by using a bi-focal optical system.
- The trigger is organized in rows.
- First and last pixel pairs of each row can be connected to the appropriate pixel pairs of the previous and the next ASICs to avoid edge effects.



Future work



- Integration of analog and digital blocks by using a digital-on-top integration flow;
- Post layout verifications;
- Tape out: early 2023;
- Test of the first prototype to obtain the performance characterization.

Submitted and published works

- Silvia Tedesco, "*A 12-bit 100 MHz SAR ADC in 110-nm CMOS for MAPSs*", SMACD/PRIME 2021, International Conference on SMACD and 16th Conference on PRIME, 2021
- Silvia Tedesco, "A Low-Power, Short Dead-Time ASIC fr SiPMs Readout with 200 MS/s Sampling Rate", 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)

Politecnico di Torino

PhD program in
Electrical, Electronics and Communications Engineering