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XXXV Cycle

Ultra low-power Interfaces for the IoT and for next-generation Biosensing

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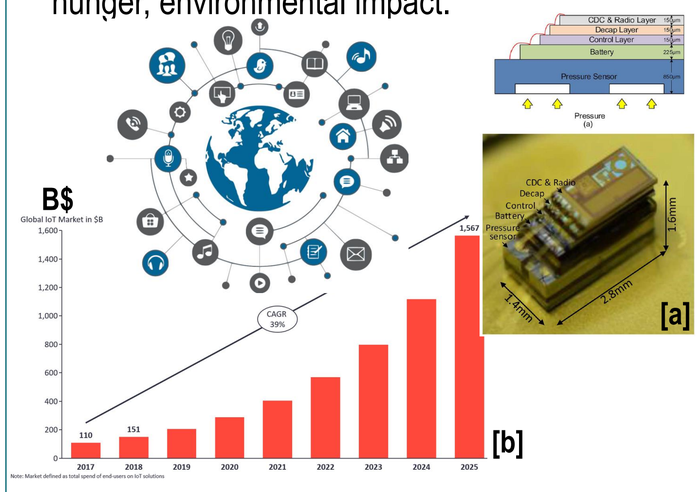
Research context and motivation

Internet-of-Things (IoT)

- Exploding number & market of IoT nodes.
- Expected market revenue 1600 **B$** by 2025
- Concerns on the maintainability, global power hunger, environmental impact.



Next-Generation Biosensing (NGB)

- Established market of wearable sensors for healthcare / telemedicine.
- Pushing towards NGB of injectable, Smart Dust, Body Dust (BD) devices.

ECG
EMG
TEMP.
SWEAT
GLUCOSE
PH

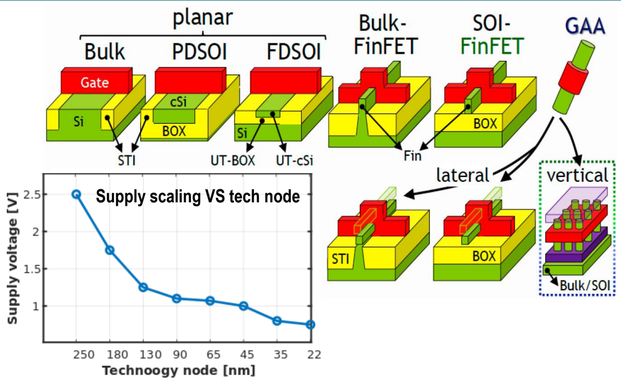
- Ultra compact, ultra low voltage (ULV), ultra low power (ULP) nodes required.
- Unregulated supply, dissipating from nW to ≈ µW power.
- Ambient-harvested energy and small, if none, battery.

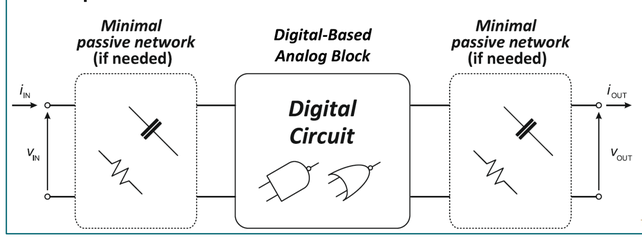
[a] S. Oh *et al.*, "A CDC Integrated in an Implantable Pressure-Sensing System," in *IEEE JSSC 2014*
[b] https://iot-analytics.com/te-q1-q2-2018-number-of-iot-devices-now-7b/
[c] "Under the skin: how insertable microchips unlock the future", The Guardian, 2017
[d] Baj-Rossi,et.al"Electrochemical biochip for applications to wireless and batteryless monitoring of free-moving mice", EMBC 2014
[e] S. Carrara, "Body Dust: Well Beyond Wearable and Implantable Sensors", IEEE Sensors Journal, June 2021

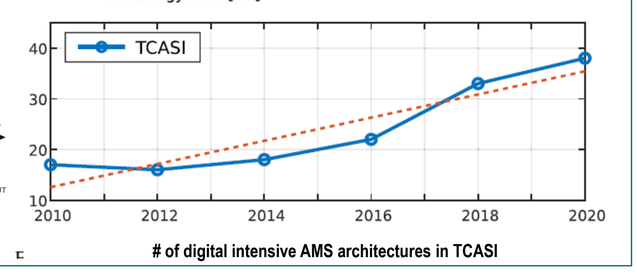
Addressed research questions/problems

ULP, ULV & low area IC constraints:

- Met in digital ICs (employing scaled techs, near threshold op., energy-quality scaling).
- Difficult to apply / not broadly applied to traditional analog design and biosignal frontends.
- Possible solution: re-think traditional analog blocks in digitally-intensive implementations.







Novel contributions

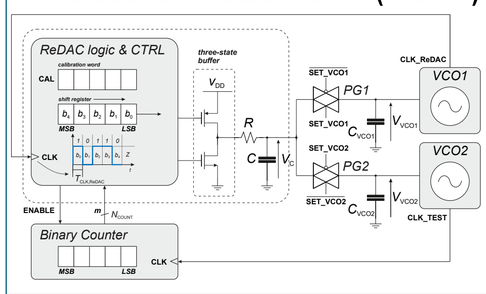
- Design and characterzation of the novel Relaxation Digital-toAnalog-Converter (ReDAC) in different implementations (40nm CMOS, 180nm CMOS, FPGA) and exploration of different calibration strategies (VCO-based, CLK-div based, DCO-based, Radix-Based Digital Correction).
- Design of Direct Digital Based Potentiostat (DDBP) for glucose detection targeting BD.
- Measures and characterization of a Digital Acquisition Front-End (DAFE) in 180nm CMOS.

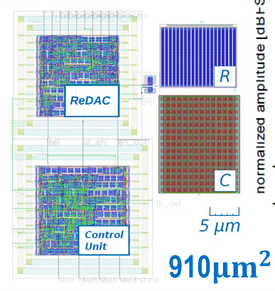
Submitted and published works

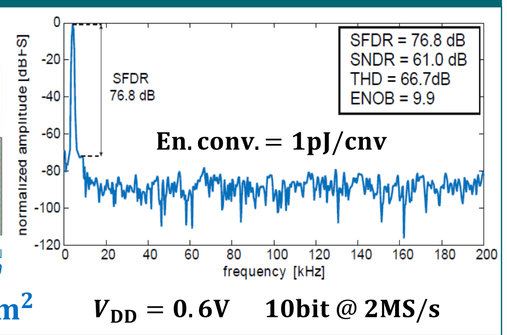
- [1] P. S. Crovetti, R. Rubino and F. Musolino, "Relaxation digital-to-analogue converter", Electronics Letters, 2019
- [2] R. Rubino, P.S. Crovetti, O. Aiello, "Design of Relaxation Digital-to-Analog Converters for Internet of Things Applications in 40nm CMOS", APCCAS 2019
- [3] P.S. Crovetti, F. Musolino, O. Aiello, P. Toledo, R. Rubino, "Breaking the boundaries between analogue and digital" IET 2019
- [4] P.S. Crovetti, R. Rubino and F. Musolino, "Relaxation Digital-to-Analog Converter with Foreground Digital Self-Calibration" ISCAS 2020
- [5] P. Toledo, R. Rubino, F. Musolino and P. Crovetti, "Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era", TCAS II 2021
- [6] R. Rubino, P. S. Crovetti and F. Musolino, "FPGA-Based Relaxation D/A Converters With Parasitics-Induced Error Suppression and Digital Self-Calibration", TCAS I 2021
- [7] R. Rubino, F. Musolino, P.S. Crovetti, "Relaxation Digital-to-Analog Converter with Radix-Based Digital Correction", ISCAS 2022
- [8] P. Crovetti, R. Rubino, et.al. "Emerging Relaxation and DDPM D/A Converters: Overview and Perspectives," 2022 MWSCAS
- [9] P.S. Crovetti, R. Rubino, P. Toledo et al. "A 0.01mm2, 0.4V-VDD, 4.5nW-Power DC-Coupled Digital Acquisition Front-End Based on Time-Multiplexed Digital Differential Amplification", ESSCIRC 2022
- [10] R. Rubino, S. Carrara, P.S. Crovetti, "Direct Digital Sensing Potentiostat targeting Body-Dust", BIOCAS 2022

Adopted methodologies

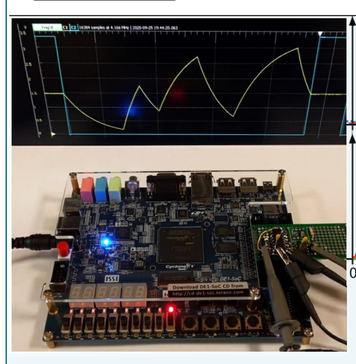
VCO-based Relaxation DAC (ReDAC) 40nm CMOS

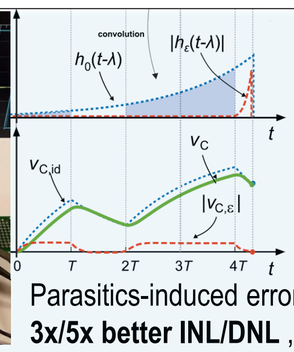






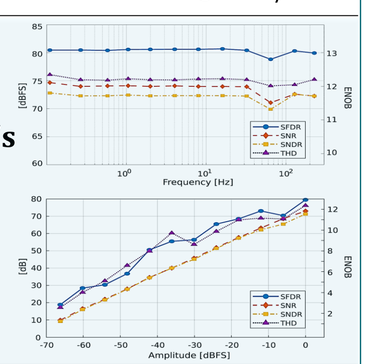
$V_{DD} = 0.6V$ 10bit @ 2MS/s



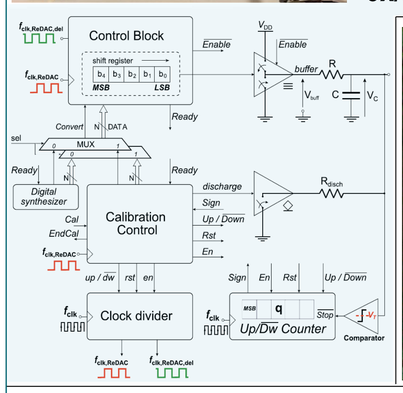


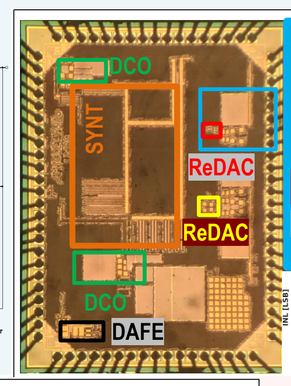
FPGA ReDAC

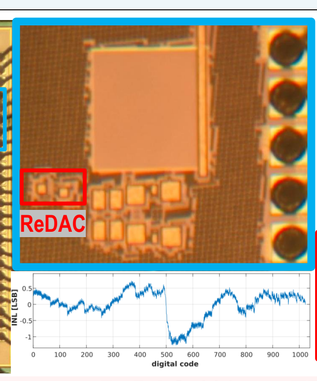
- **13bit @0.5kS/s**
- **10bit @10.5kS/s**
- **6 logic elements** (2000x less than ΣΔ 9x less than DDPM)

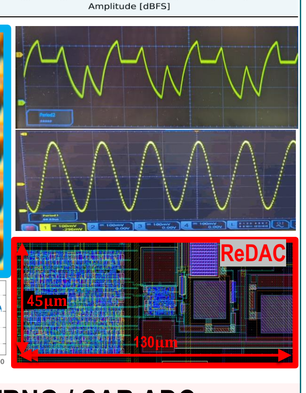


Parasitics-induced error Suppression:
3x/5x better INL/DNL , 3 more ENOB ☺

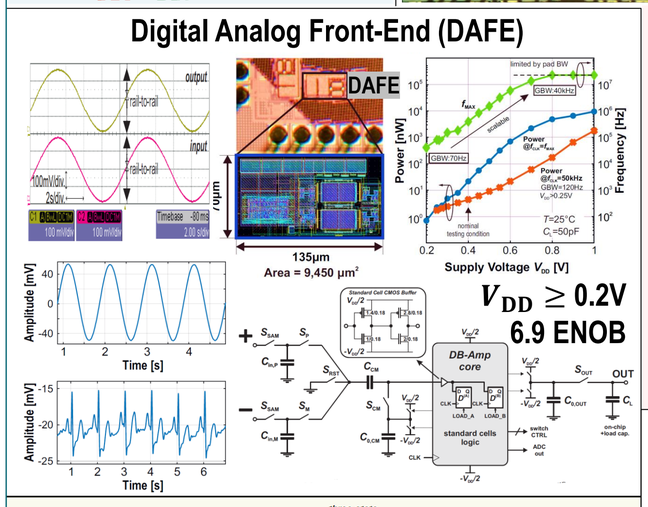






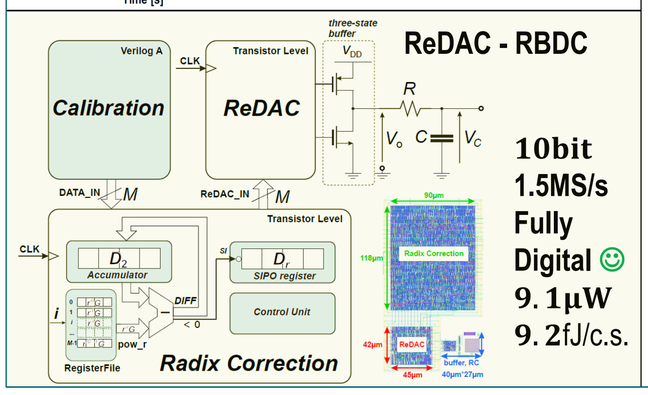


Digital Analog Front-End (DAFE)



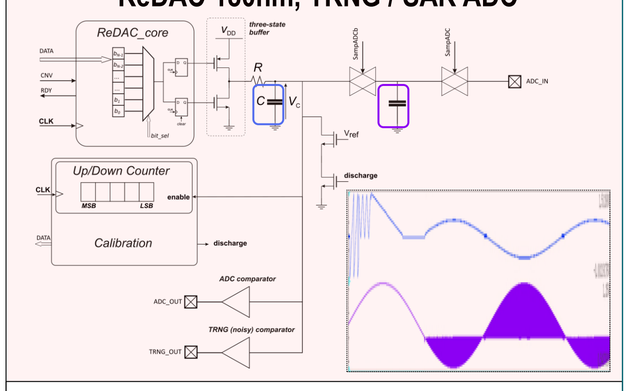
$V_{DD} \geq 0.2V$
6.9 ENOB

ReDAC - RBDC

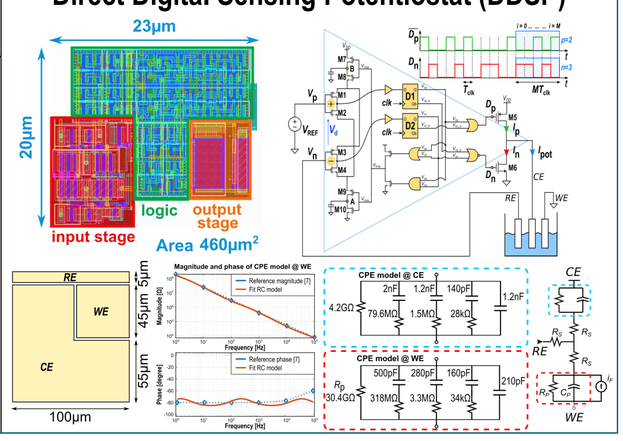


10bit
1.5MS/s
Fully Digital ☺
9.1µW
9.2fJ/c.s.

ReDAC 180nm, TRNG / SAR ADC



Direct Digital Sensing Potentiostat (DDSP)



Future work

- Expand the research on ReDAC and the Digital-Based Approach towards applications such as ΣΔ ADCs, BD potentiostat reference for CA and CV, Virtual Voltage References.
- Prototype and characterize Next-Generation Biosensing frontends (Electrochemical Sensors, ECG, EMG) and validate electro-chemical interface electrical models.

List of attended classes

- 01UJBRV - Adversarial training of neural networks (3/6/2021, 3)
- 01UMNRV - Advanced deep Learning (didattica di eccellenza) (15/6/2021, 6)
- 01QTXRV - BIO/CMOS interfaces and co-design (31/8/2021, 3)
- 01RISRV - Public speaking (21/1/2022, 1)
- 01SWQRV - Responsible research and innovation, the impact on social challenges (29/4/2022, 1)
- 01SYBRV - Research integrity (20/5/2022, 1)
- 01SWPRV - Time management (20/5/2022, 1)
- 02RHORV - The new Internet Society: entering the black-box of digital innovations (21/05/2022, 1)
- 01UNVRV - Navigating the hiring process: CV, tests, interview (23/5/2022, 1)
- 01UNYRV - Personal branding (25/05/2022, 1)
- 01SHMRV - Entrepreneurial Finance (28/5/2022, 1)
- 01DMJRV - Design Thinking, Processes and Methods (10/6/2022, 0.4)
- 08IXTRV - Project management (15/7/2022, 1)

Politecnico di Torino

PhD program in

Electrical, Electronics and Communications Engineering