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XXXV Cycle

VLSI Architectures for Video Processing and RISC-V implementations

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Research context and motivation

Video Processing

- **Research Area:**
  - Image processing, Visual object tracking, VLSI based architectures
- **Motivation:**
  - Huge amount of data processing
  - Computer based solutions are slow
  - Need fast solution for operating in real time
  - Hence hardware acceleration
- **Applications:**
  - Surveillance, Robotics, VAR, Road Scene understanding e.t.c.

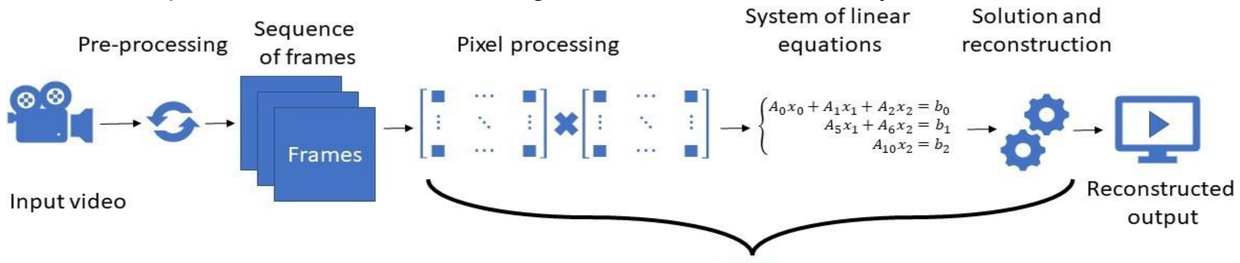
RISC-V

- **ResearchArea:**
  - Processor design, VLSI.
- **Motivation:**
  - Multi-core processors are the new paradigms for performance
  - Dependencies are a limiting factor for increasing performance
  - Memory hierarchy for fast access time
  - Tomasulo's architecture
- **Applications:**
  - Modern PCs, Research platforms e.t.c.

Addressed research questions/problems

- **Research Problem 1:**

Video usage has become elementary in communication which has made its use in a higher number of devices. Moreover, higher resolution videos have led to more memory usage and data compression achieved via video coding techniques. Thus, the goal is to obtain an implementation of video coding to share videos fast, easy and at low cost.

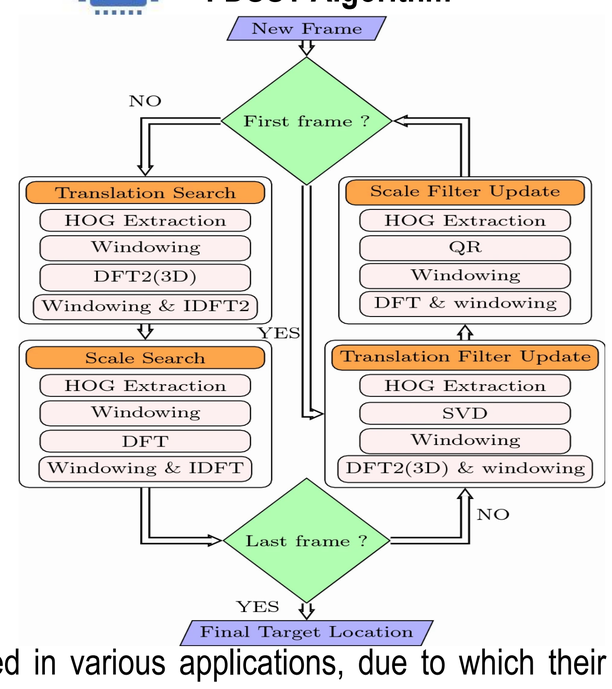


Wiener Filter

- **Research Problem 2:**

Real-time object tracking in videos is vital in many image processing applications. For this, efficient hardware architectures must achieve the desired accuracy while satisfying the frame rate requirements. The existing visual tracking methods employ sophisticated algorithms and challenge the capabilities of most embedded architectures. Fast Discriminative scale space tracking (FDSST) is one algorithm that can demonstrate adequate performance with affordable complexity.

FDSST Algorithm



- **Research sub-topic:**

High-performance processors are used in various applications, due to which their area and power optimization lead to different solutions. The Out-of-Order (OoO) execution is essential for achieving high performance. New processor Instruction Set Architecture (ISA) called RISC-V is open source and modular, making it easier to implement and extend for many applications than closed and incremental ISA. Thus, the VLSI implementation of the OoO RISC-V processor called LEN5 is presented as a scalable research platform with competing performance and area.

Submitted and published works

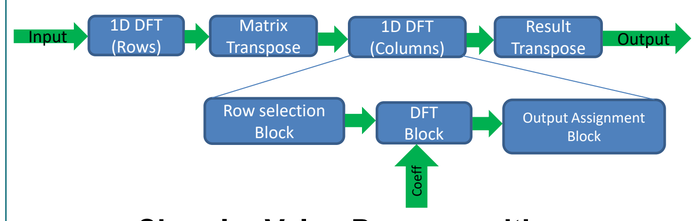
- Walid, W. , Awais, M., Ahmed, A., Masera, G., and Martina, M., "*Real-time implementation of fast discriminative scale space tracking algorithm*", Journal of Real-Time Image Processing, vol. 18, no. 6, 2021, pp. 2347-2360
- Walid, W. , Armando, G., Di Paola, S., Ruo Roch, M., Masera, G., Martina, M., "*VLSI Architectures of a Wiener Filter for Video Encoding*", MDPI Electronics, vol. 10, no. 16, 2021, pp. 1961

Novel contributions

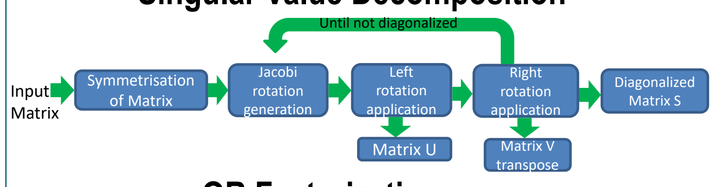
- The presented work provides an algorithm-to-architecture mapping of the Wiener Filter for AOMedia AV1 video coding. In terms of throughput, the solution is much better than the state-of-the-art. The proposed solution via optimizations allows the Wiener filter to achieve a 100× reduction in processing time compared to existing works and a 5× improvement in Mega samples per second.
- A careful design exploration of core mathematical operations of the tracking algorithm is performed to improve their hardware utilization and timing performance. Among the core functional units optimized in this work, the discrete Fourier transform achieves a computational time improvement of 92% relative to existing works, QR factorization achieves a 2.3× reduction in resource utilization, and singular value decomposition yields a 3.8× improvement in processing time. Furthermore, for an input image size of 320 × 240, the proposed architecture achieves a mean of 25.38 fps.
- A 6-stage RV32/64I OoO RISC-V core with distributed control operating at high frequency.

Adopted methodologies

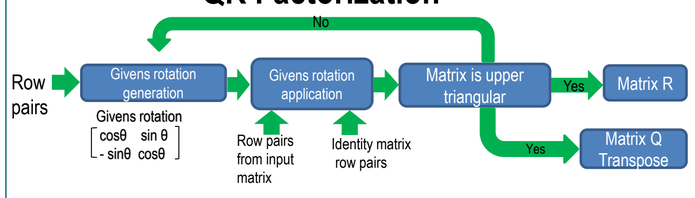
FDSST: DFT2



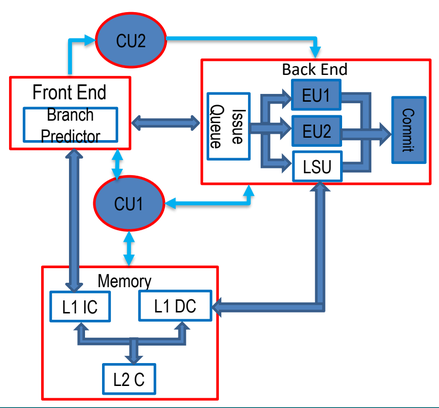
Singular Value Decomposition



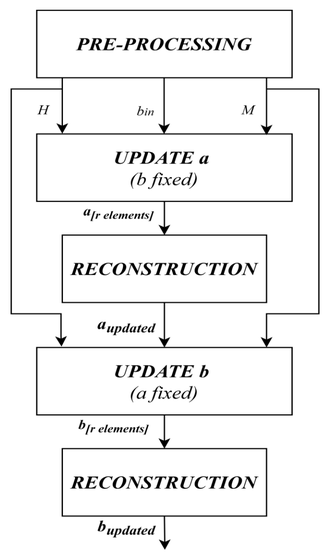
QR Factorization



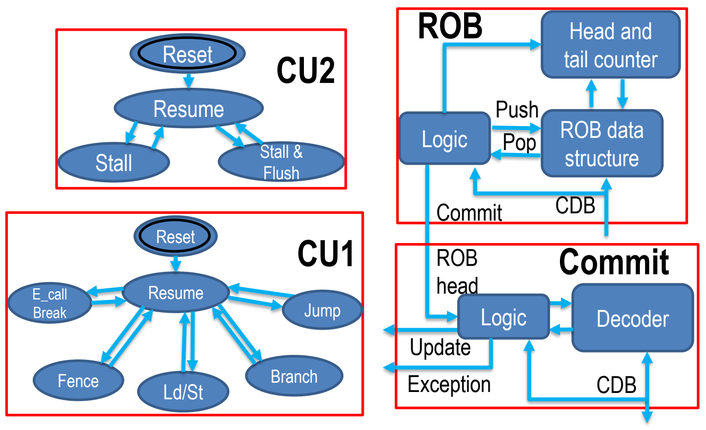
LEN5 block diagram



Wiener Filter: Datapath



LEN5 control and commit



Future work

- Future works include the overall power and accuracy analysis of the implemented Wiener filter relative to the literature.
- Future research on FDSST architecture is to optimize further the operations involved. An effort can also be made to integrate the whole algorithm implementation and interface with a real camera to test it in the field. Finally, the overall accuracy of the algorithm can be compared to the databases available.
- For LEN5, the inclusion of other ISA extensions and benchmarking.

List of attended classes

- 01QSBIU – Formal verification of concurrent and distributed software and systems (15/07/2021, 20 credits)
- 01SHORV – Nano & Quantum Computing (16/12/2021, 40 credits)
- 01RGBRV – Optimization methods for engineering problems (15/06/2020, 30 credits)
- 01MNFIU – Parallel and distributed computing (22/07/2020, 25 credits)
- 01UIYRV – Physics-based modeling of semiconductor devices (01/04/2020, 15 credits)
- 01DUCRV – Principles of digital image processing and technologies (29/7/2022, 27credits)
- 01QSCIU – Reconfigurable computing (20/07/2020, 20 credits)
- 01QORRV – Writing Scientific Papers in English (26/03/2020, 15 credits)

Politecnico di Torino

PhD program in
Electrical, Electronics and Communications Engineering