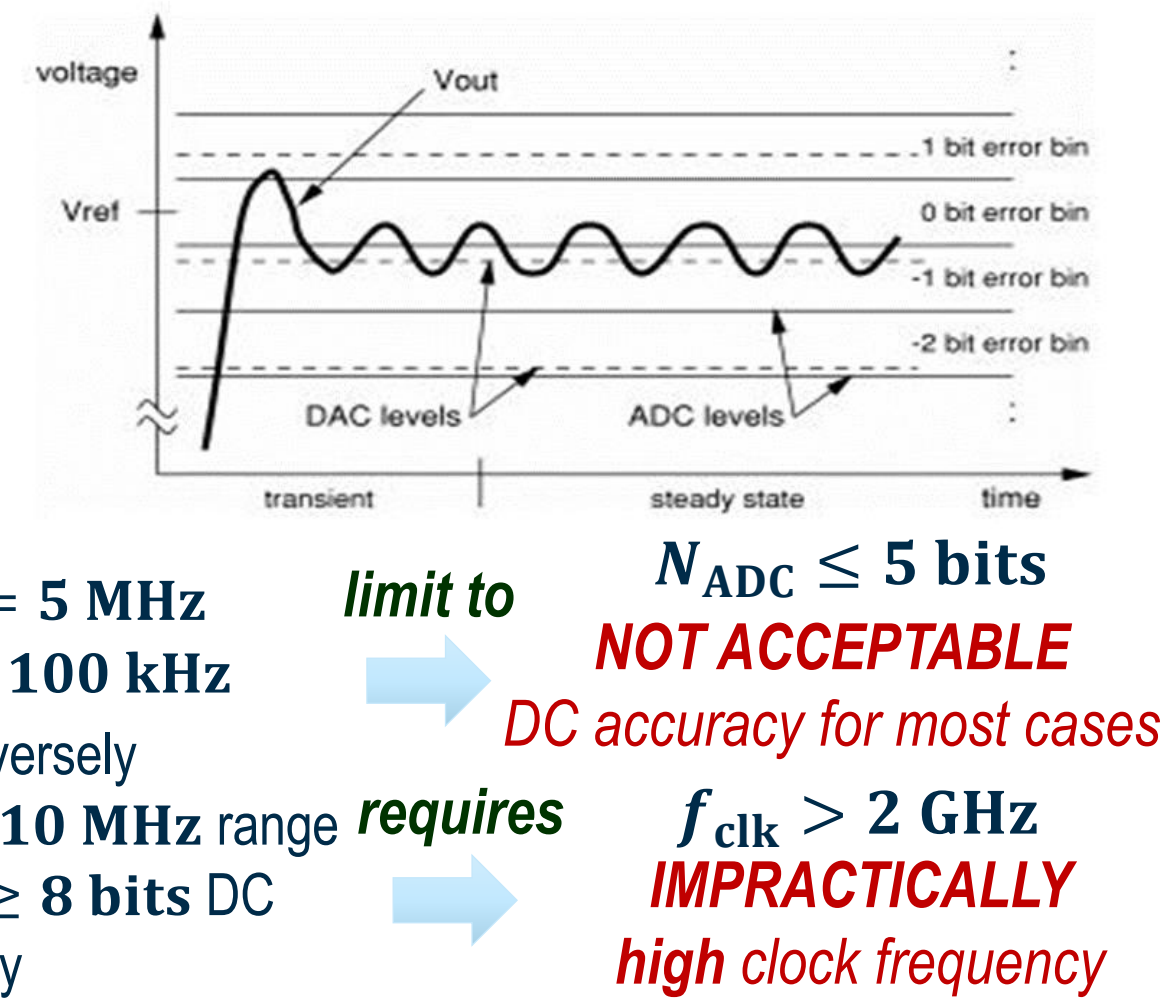
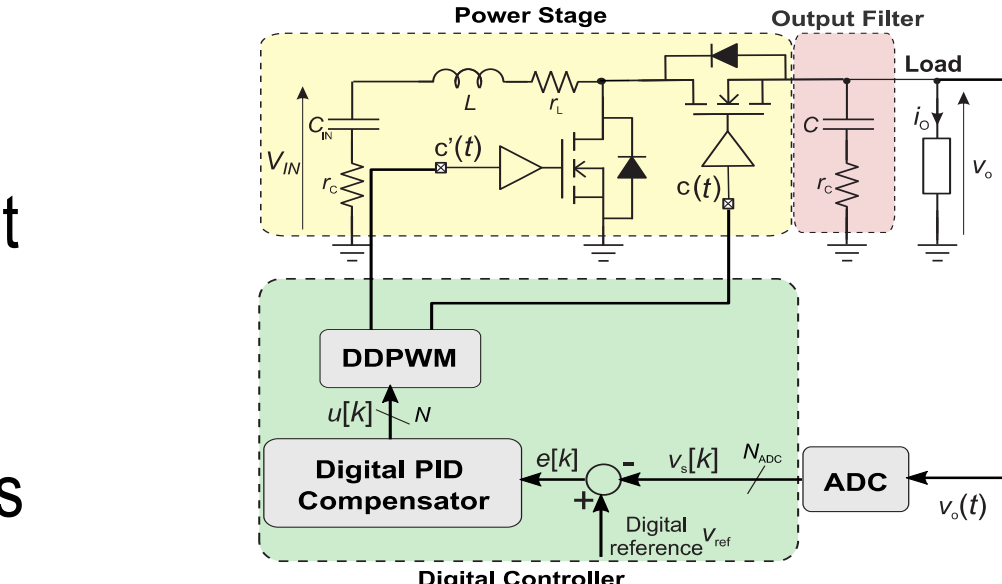


## Research context and motivation

### ❖ Limit-cycle Free, Digitally Controlled Boost Converter based on DDPWM

- Digital controllers are more prevailing in switching-mode power converters
- flexibility, reliability, good performance, low cost and reduced susceptibility to aging.
- Boost converter used in photovoltaic systems, in battery powered and portable device applications



- Spectral characteristics of DDPWM
- baseband digital-to-analog (D/A) conversion
- digital-based operational transconductance amplifiers
- analog-to-digital (A/D) conversion
- digitally-controlled power converters
- DDPM is area and power-efficient
- all-digital hardware implementation
- Limit-cycle Oscillations (LCOs)
- To remove LCOs,  $N_{DDPM} > N_{ADC}$
- a) Requires high clock frequency
- b) Limited DC accuracy.

### ❖ Design and efficiency analysis of an LCL capacitive power transfer system with load-independent ZPA

- Capacitive based wireless Power Transfer CPT

References:  
 [1] M. Usmonov, P. S. Crovetto, F. Gregoretti and F. Musolino, "Suppression of Quantization-Induced Limit Cycles in Digitally Controlled DC-DC Converters by Dyadic Digital Pulse Width Modulation," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 2224-2231, doi: 10.1109/ECCE.2019.8913214.  
 [2] P. S. Crovetto, M. Usmonov, F. Musolino and F. Gregoretti, "Limit-Cycle-Free Digitally Controlled DC-DC Converters Based on Dyadic Digital PWM," in IEEE Transactions on Power Electronics, vol. 35, no. 10, pp. 11155-11166, Oct. 2020, doi: 10.1109/TPEL.2020.2978696.

## Addressed research questions/problems

### ❖ Limit-cycle Free, Digitally Controlled Boost Converter based on DDPWM

- Sigma-Delta ( $\Sigma\text{-}\Delta$ ) modulation, multiphase PWM, digital thermometric dithering (DTD)
- Dyadic digital PWM (DDPWM)
- a) DDPWM is implemented on FPGA
- b) effective for LCO-free operation in a buck converter
- Buck converter  $V_o = V_{in} \cdot D$ , while boost converter  $V_o = V_{in} / (1 - D)$
- So, finer quantization steps at lower duty-cycle and coarser steps as duty-cycle increases.

### ❖ Software-defined DDPWM Modulators in General Purpose Microcontrollers

- Significant attention to digital HW implementation
- SW implementation in a microcontroller HW has not been specifically addressed

### ❖ LCL capacitive power transfer system with load-independent ZPA

- desirable feature in battery charger is the zero-phase angle (ZPA)
- ZPA operation must be load independent

## Novel contributions

### ❖ Limit-cycle Free, Digitally Controlled Boost Converter based on DDPWM

Dyadic Digital Pulse Width Modulation

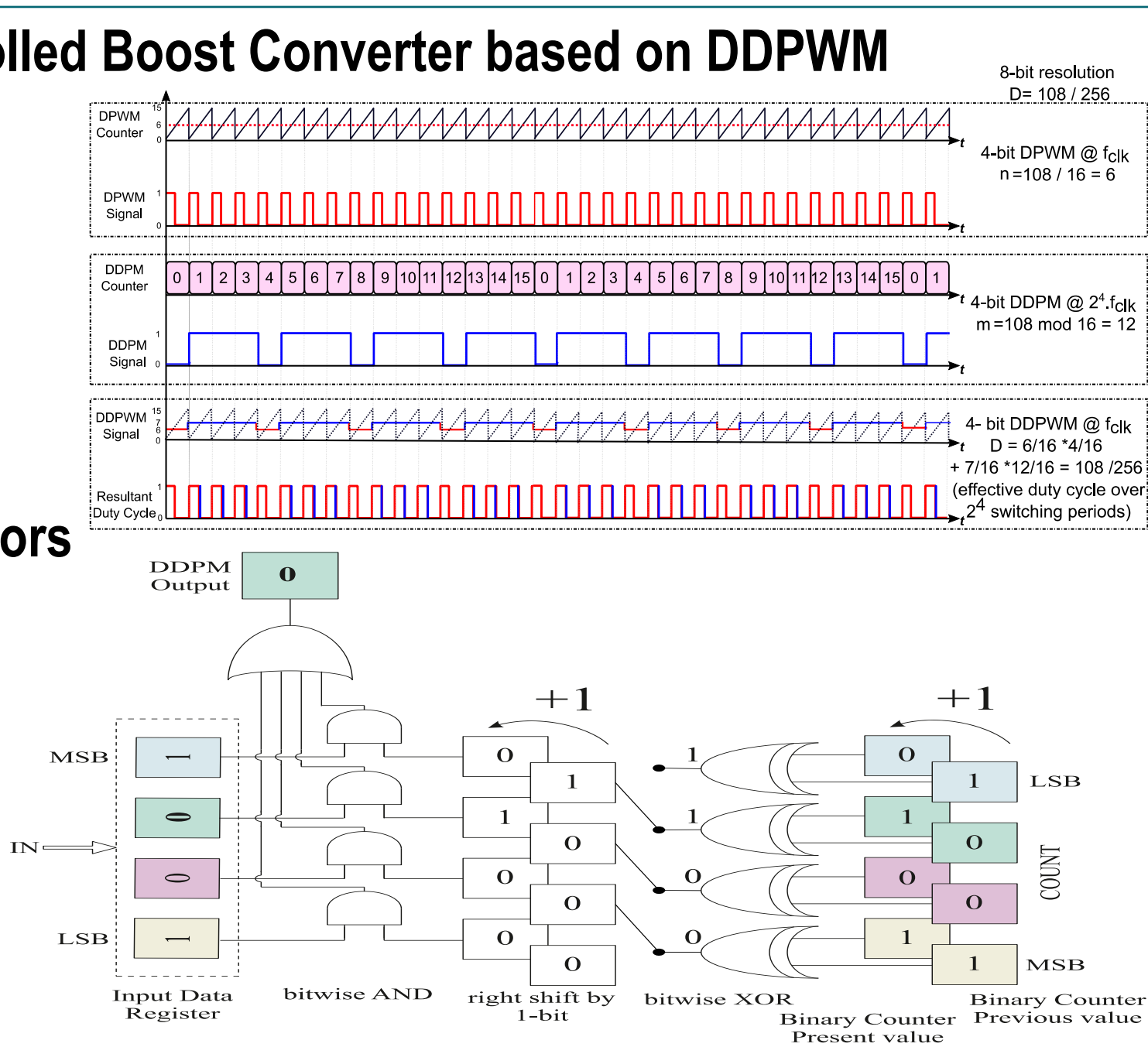
- New and deterministic approach
- Effectively increase the DPWM resolution

- Spurious spectra pushed at high frequency

### ❖ Software-defined DDPWM Modulators in General Purpose Microcontrollers

- New DDPWM modulator architecture
- amenable to SW implementation on microcontroller.

- Compared to SW architecture resulting from straightforward translation of HW implementation.



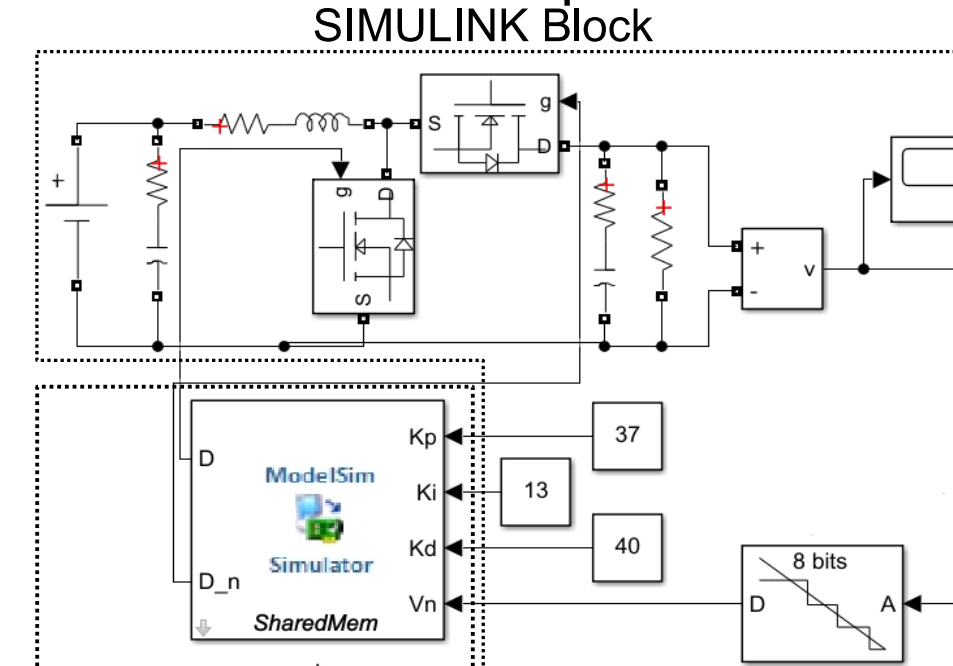
## Submitted and published works

- A. Abdullah, F. Musolino and P. Crovetto, "Software-Defined DDPWM Modulators for D/A Conversion by General-Purpose Microcontrollers," in IEEE Access, vol. 10, 2022, pp. 17515-17525
- P. Crovetto, R. Rubino, A. Abdullah and F. Musolino, "Emerging Relaxation and DDPWM D/A Converters: Overview and Perspectives," 2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS), 2022, pp. 1-6
- Francesco Musolino, Ahmed Abdullah, Mario Pavone, Fabio Ferreyra, Paolo Crovetto, "Design and efficiency analysis of an LCL Capacitive Power Transfer system with Load-Independent ZPA," EPE'22 ECCE Europe, 2022
- A. Abdullah, F. Musolino and P. Crovetto, "Limit-Cycle Free, Digitally-Controlled Boost Converter based on DDPWM," in IEEE Access (to be submitted)

## Adopted methodologies & Results

### ❖ Limit-cycle Free, Digitally Controlled Boost Converter based on DDPWM

#### • Co-simulation setup



#### • Design Specifications

Param.	Val.	Unit	Param.	Val.	Unit
$C_o$	3	$\mu\text{F}$	$V_{in}$	7-10	V
$R_L$	25-30	$\Omega$	$V_o$	13.8	V
$L$	900	nH	$f_{sw}$	1.17	MHz

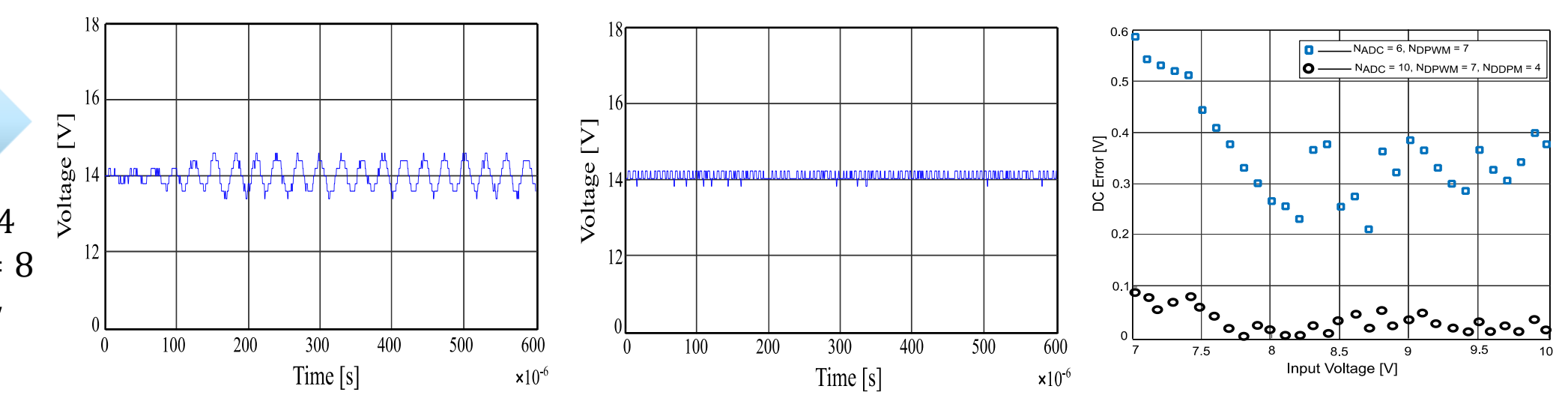
#### • Results

##### i. No LCOs

$N_{Adc} = 5, N_{DDPM} = 4$

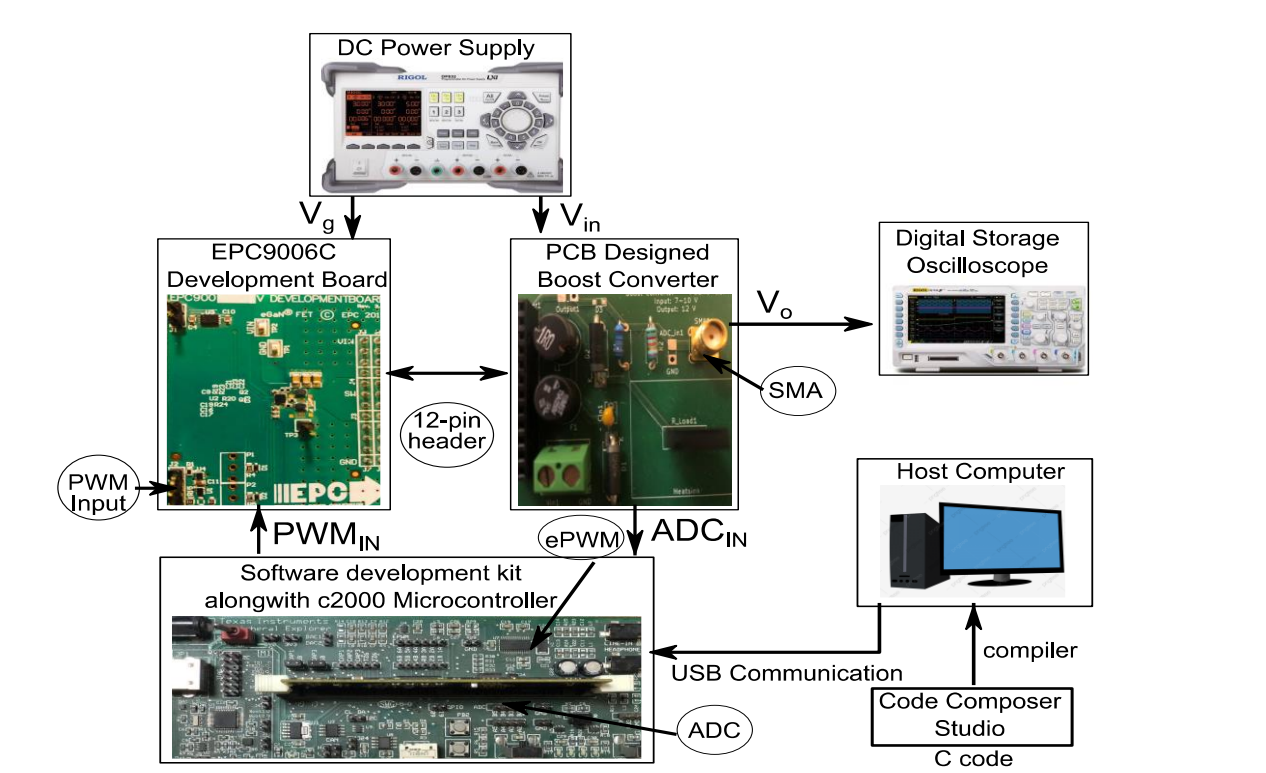
$N_{Adc} = 5, N_{DDPM} = 8$

##### i. DC accuracy



#### • Experimental Test Setup

- C2000 microcontroller board with onboard ADC and PWM modules
- Algorithm is programmed in C-language
- PCB designed boost converter
- EPC9006C board



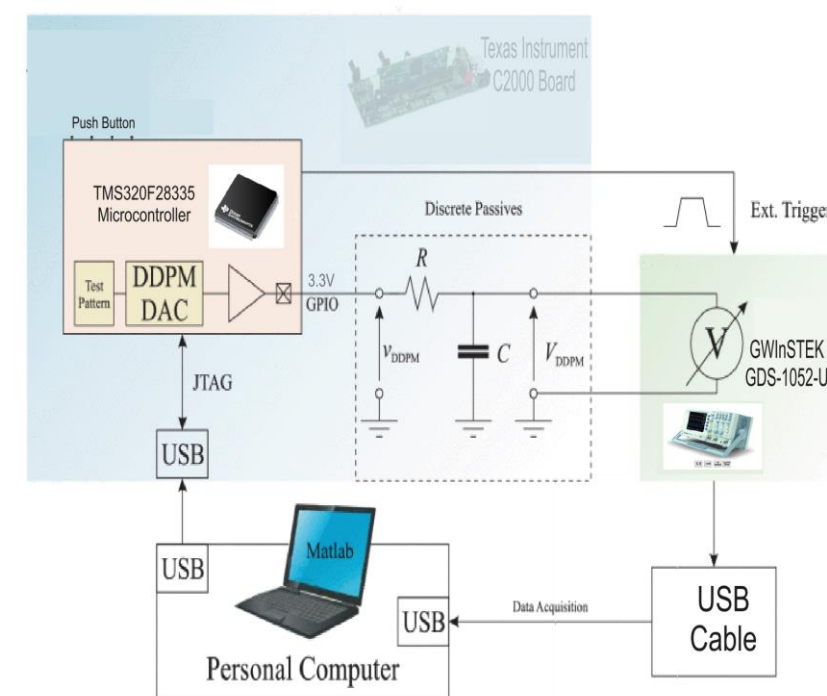
### ❖ Software-defined DDPWM Modulators in General Purpose Microcontrollers

#### • Experimental Test Setup

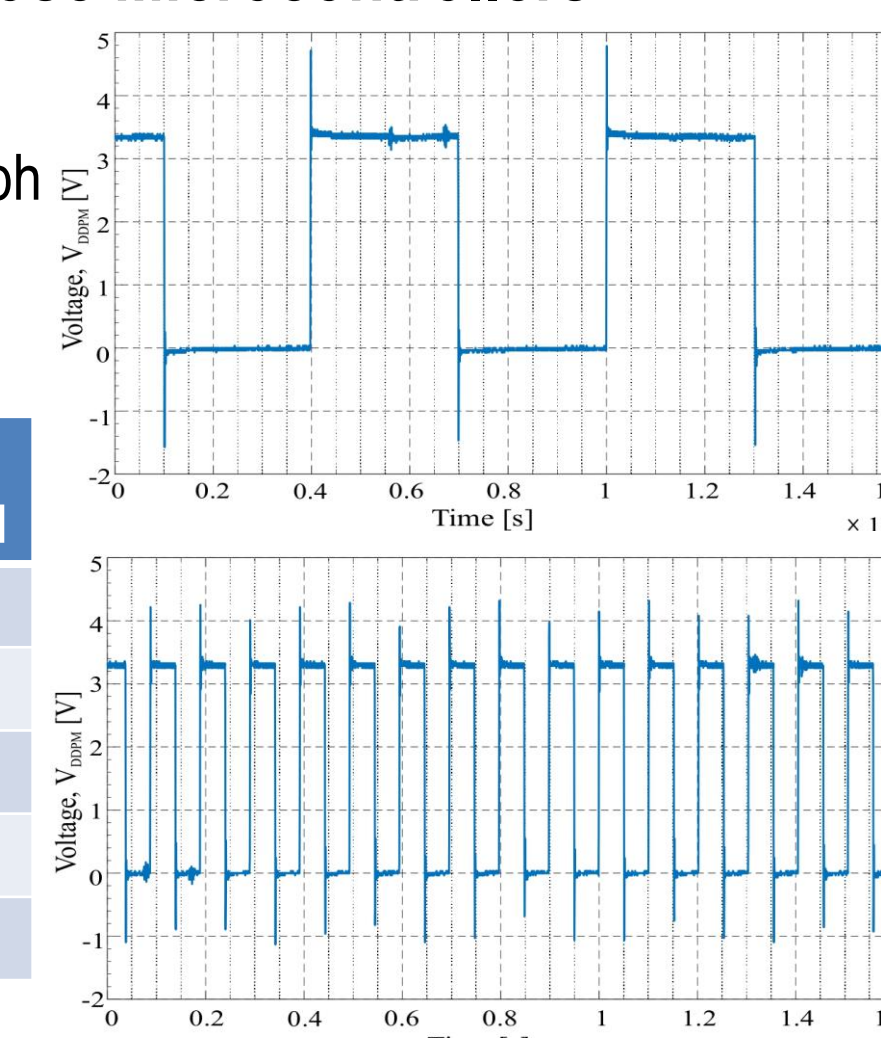
- 8-bit DDPWM DAC on c2000 microcontroller
- low-pass RC filter

#### • Results

- Maximum Pulse time graph
- Static characteristics
- Dynamic characteristics



Param.	Unit	Prop. DDPWM	Iter. DDPWM
INL	LSB	1.64	2.8
DNL	LSB	1.79	3.53
SNDR	dB	45.27	41.61
SFDR	dB	47.02	45.16
ENOB	Bit	7.23	6.62

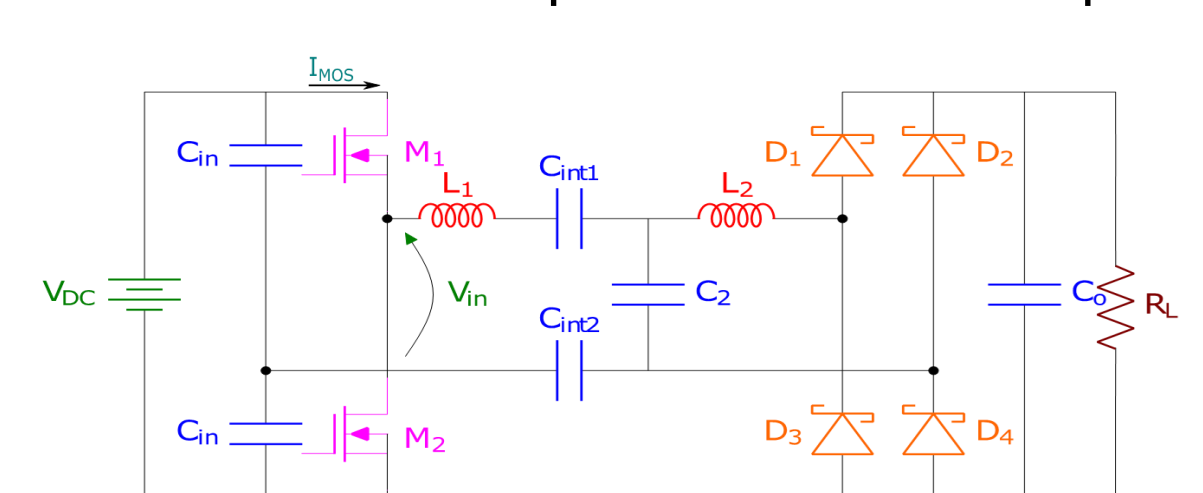


### ❖ LCL capacitive power transfer system with load-independent ZPA

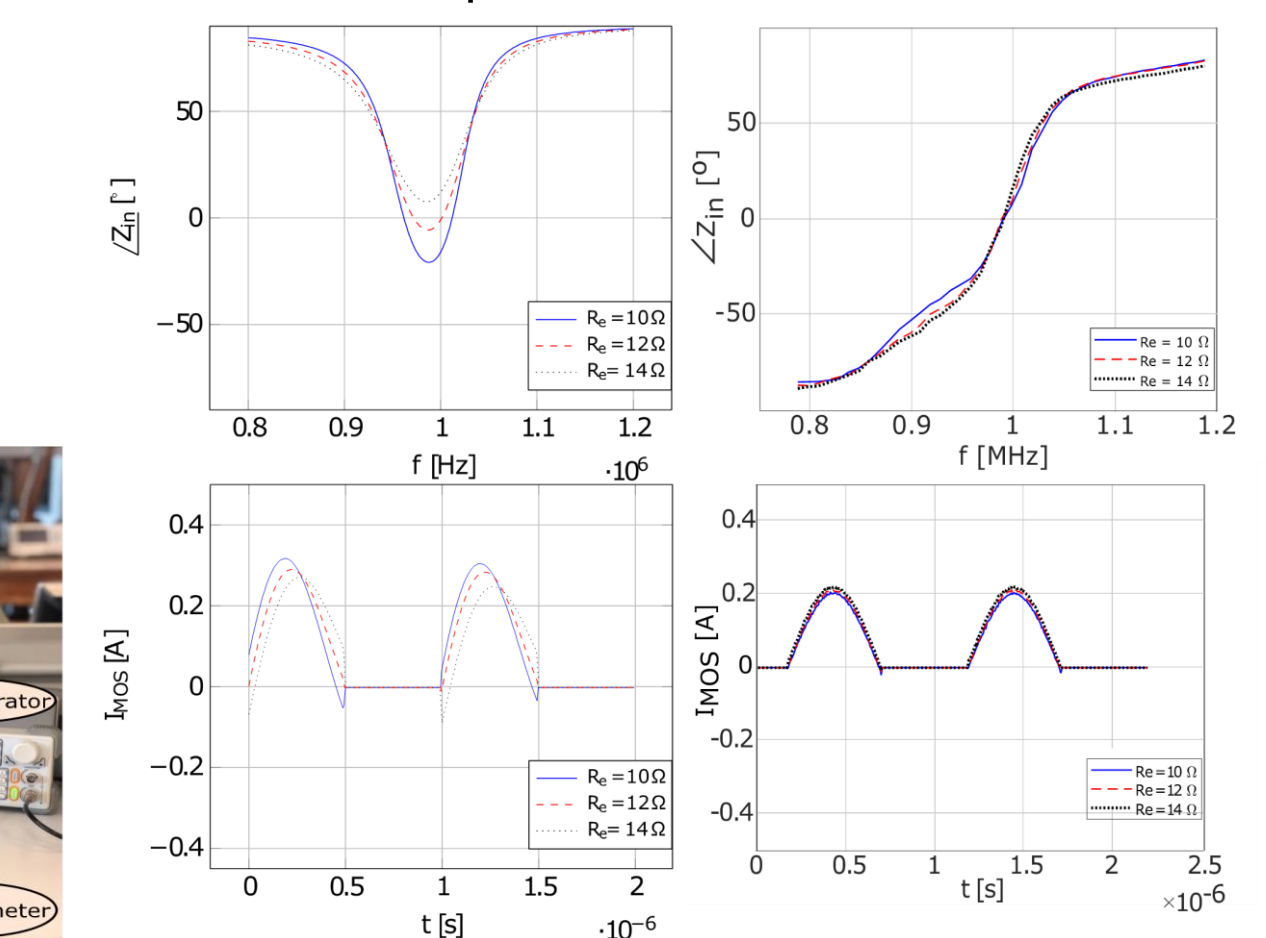
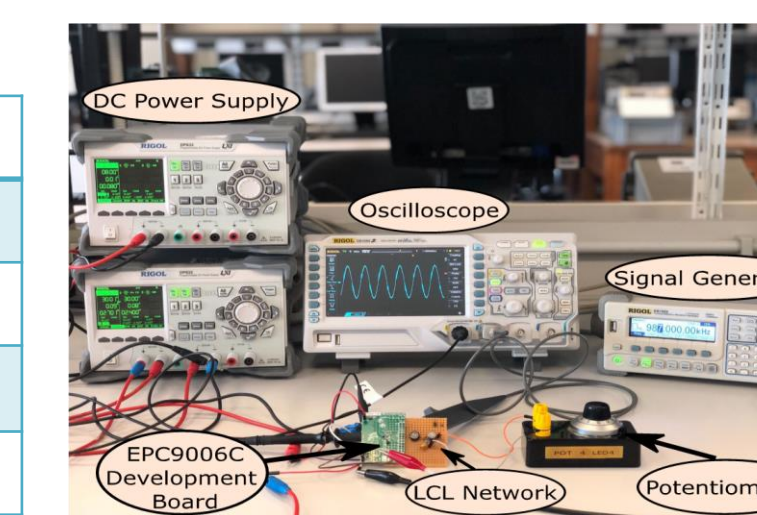
#### • Schematic and Experimental test setup

#### • Results

Load-independent ZPA



Comp.	Value
$L_1$	470 $\mu\text{H}$
$L_2$	10 $\mu\text{H}$
$C_{int1,2}$	100 pF
$C_2$	2.7 nF



## Future work

### ❖ Limit-cycle Free, Digitally Controlled Boost Converter based on DDPWM

- In preparation to be submitted to IEEE Access
- Expand the research in the digitally controlled converter to limit the onset of LCOs
- Thesis writing and attend courses
- Collaborate with Prof. Francesco Musolino in conducting Power Electronics Lab

## List of attended classes

- 01DNZRV – Emerging Ultra-low Voltage, Ultra-low Power Analog and Mixed-Signal Integrated Circuits for the IoT (06-22, 4)
- 01RGRV – Optimization methods for engineering problems (07-06-22, 6)
- 01DMQRV – Power electronics for grid applications (06-22, 4)
- 08IXTRV – Project management (04-22, 1)
- 01QAAAA – Public speaking (04-22, 1)