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XXXVII Cycle

Towards Accelerated Transient Solvers For Power Integrity Verification

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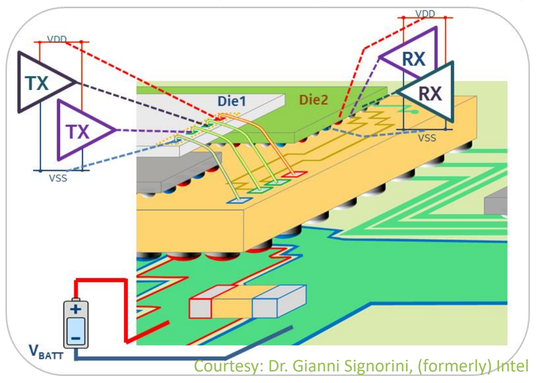
Research context and motivation

Context

- Design and verification of large-scale VLSI systems largely relies on repeated **system-level simulations.**
- Transient simulations are computationally expensive, hence the need for modeling and simulation algorithms yielding reliable results much faster than a traditional circuit solver.
- A model reduction and simulation framework tailored for **full-system power delivery networks** is still a gap we aim to fill.

Application-driven

- Recently, **Fully-Integrated Voltage Regulators (FIVR)** have been introduced in microprocessors to enable finer control over power domains and balance performance and power usage.
- Our application is a system made up of a power delivery network at the board, package and die levels along with integrated buck regulators. In particular, **FIVR**s render established approaches for LTI systems modeling unsuitable, requiring novel solutions.



Courtesy: Dr. Gianni Signorini, (formerly) Intel

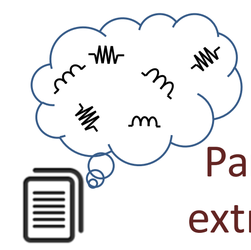
Addressed research questions/problems

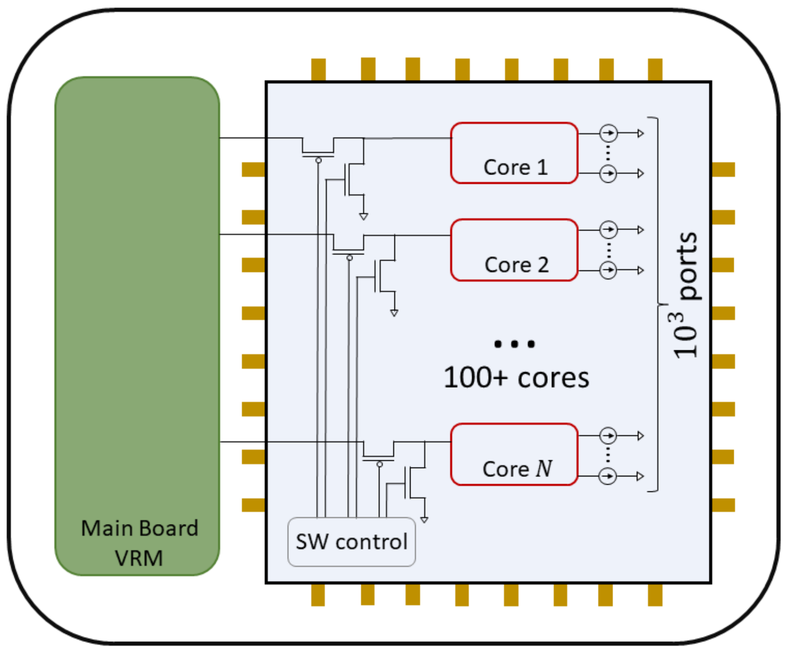
In collaboration with **Intel**, we develop a **fast transient solver** specifically geared towards power delivery networks of many-core processors including on-chip voltage regulation via integrated buck converters. **Full system-level PDN verification is not feasible with state-of-the-art simulation software**. To this aim, we address the following research problems:

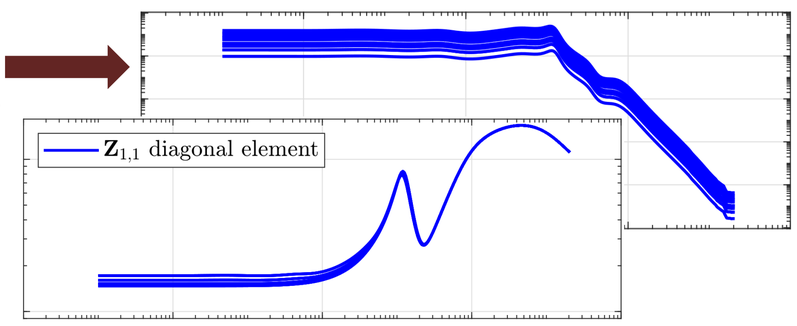
- **Model reduction of electrical networks** with **high dynamic order** and **port count**, including mildly nonlinear or switching devices.
  - Large-scale MOR approaches for the PDN+regulator system with controlled accuracy.
  - Symmetric multicore structures offer potential for model compression that has not been fully explored yet.

- Development of **parallel algorithms for transient analysis** leveraging parallel computing (GPUs, multi-processing) in circuit-level simulation.
  - How can we partition a large-scale network for efficient parallel simulation?
  - Can we exploit the heterogeneity of components involved to apply multi-rate integration methods?

- **Data-driven macromodeling** of many-port systems to enable seamless integration of data acquired from field solvers into a circuit-oriented simulation.

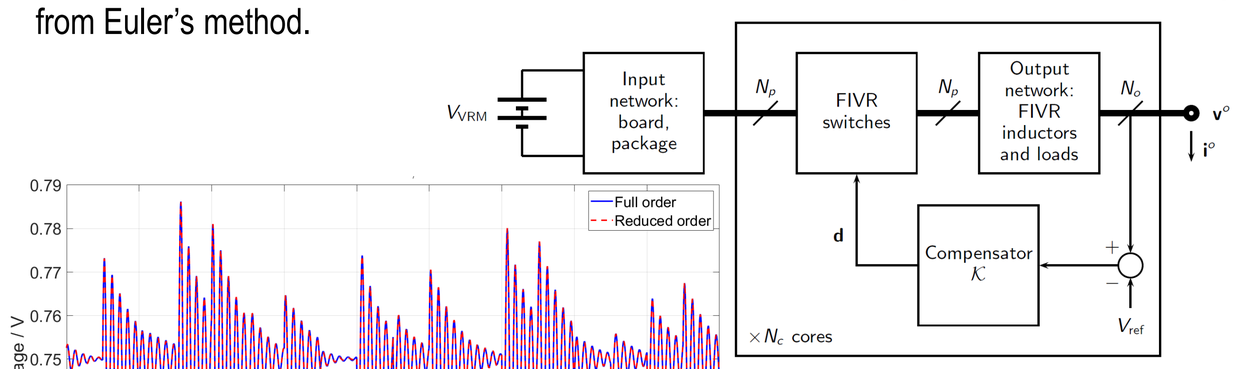

Parasitic extraction
+
Field simulations

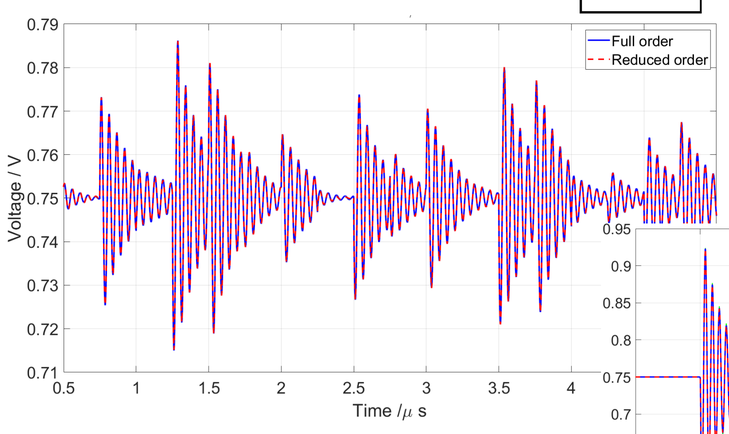


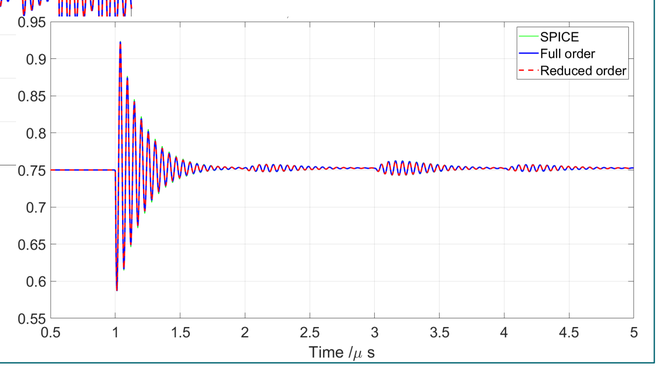


Novel contributions

- Application of data-driven **parametrized macromodeling** to represent a set of linear systems indexed by a **time-varying parameter**. This idea allows to recast the nonlinearity introduced by the buck converter as a linear parameter-varying (LPV) system.
- Formulation and implementation of **mixed implicit-explicit integration method**, starting from Euler's method.





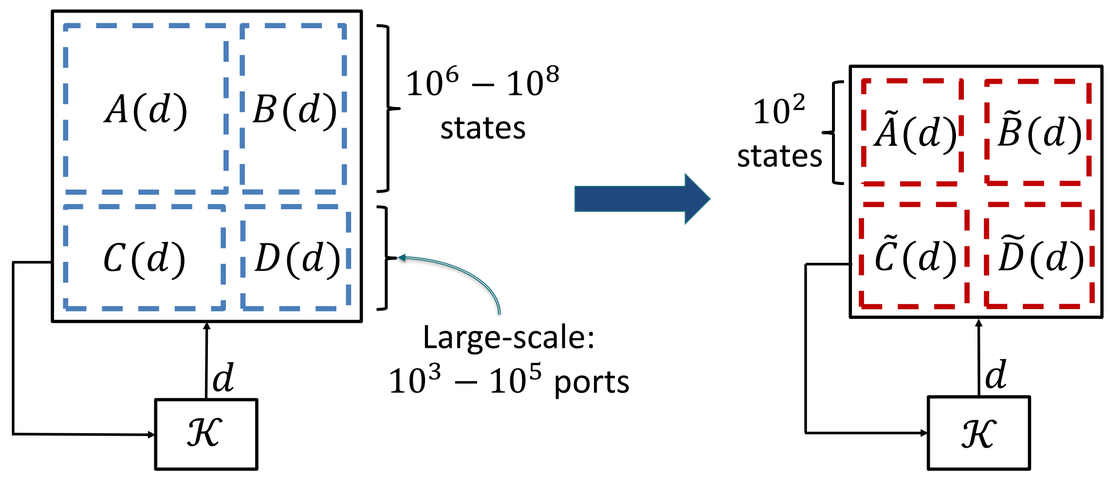


10-100x speedup

Adopted methodologies

- **Data-driven** rational **macromodeling** algorithms, such as Vector Fitting (VF), to integrate field simulation data in lumped circuit descriptions.
- **Linear parameter-varying** system theory, for modeling buck regulator dynamics coupled with the power delivery network.
- **Parametrized macromodeling**, as a framework to represent **switching**, **nonlinear** or **time-varying** systems.
- **TBR** and **Krylov subspace** methods for model reduction.

$$\dot{x} = A(d(t))x + B_o(d(t))i^o + B_i(d(t))V_{in}$$
$$y = C(d(t))x + D_o(d(t))i^o + D_i(d(t))V_{in}$$
$$\dot{w} = A_k w + B_k e$$
$$d = C_k w + D_k e$$



Future work

- Development of **model reduction** methods suited for **large-scale** systems with **switching** or **mildly nonlinear** components.
- Leverage the highly symmetric and repetitive structure typical of a multi-core processing system to derive a **compressed representation** of the system's responses.
- Devise a **parallel circuit simulation** algorithm that is scalable to large systems, possibly exploiting the computing capabilities of GPUs.

Submitted and published works

- A. Carlucci, S. Grivet-Talocia, S. Mongrain, S. Kulasekaran, K. Radhakrishnan "Towards Accelerated Transient Solvers for Full System Power Integrity Verification", EPEPS 2022, accepted for publication
- A. Carlucci, A. Zanco, R. Trinchero, and S. Grivet-Talocia, "Vector Fitting of Noisy Frequency Responses via Smoothing Regularization," in 2022 IEEE 26th Workshop on Signal and Power Integrity (SPI), Siegen, Germany, May 2022, pp. 1–3.

List of attended classes

- 01TXFSM – Machine Learning And Deep Learning (20/7/2022, 10 CFU)
- 02SFURV– Programmazione scientifica avanzata in Matlab (26/5/2022, 6 CFU)
- 01RGBRV – Optimization methods for engineering problems (7/6/2022, 6 CFU)
- 01TUFRV– Research Data Management and Open Access Publishing (12/4/2022, 3 CFU)
- 01PJMRV – Etica Informatica (27/4/2022, 4 CFU)
- MLCC22: Machine Learning Crash Course (1/7/2022, 24 hrs)
- HiDaDeeL: High-Dimensional Approximation and Deep Learning (20/5/2022, 24 hrs)

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